Ultra-High-Speed A/D Converter Based on Resonant-Tunneling Diodes

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Final R&D Report

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Executive Summary

Future DoD requirements for RF and microwave systems for signal processing, communications, digital beam-forming, etc., mandate the development of high-speed A/D converters. While conventional flash A/D converters have potential for high speed operation, they are highly complex circuits and are power hungry. In this program, we proposed and demonstrated a new approach to an A/D converter using resonant tunneling diodes (RTDs) which operate at higher speeds than conventional flash A/Ds and which are potentially much lower in complexity, power consumption and manufacturing cost. The achievement of a fully functional 5 bit A/D was by far the most significant accomplishment of this program. It proved unequivocally that our basic concept for the RTD-based A/D worked. It also demonstrated that the selective epitaxial process we developed for integrating InP-based RTDs and MODFETs is a viable technology. It showed that we developed an overall process which produced working circuits. Moreover, our SPICE models for these RTDs are suitably accurate for designing and simulating circuits.

The overall objective of this program was to demonstrate the feasibility of monolithic, 3- and 6- bit A/D converters with effective sampling rates of 10 and 4 GHz, respectively. The program had three phases.

During Phase I of this program, we developed a selective epitaxial process for monolithically integrating GaInAs/AlInAs modulation doped field effect transistors (MODFETs) and RTDs via MBE on an InP substrate. We were able to integrate these two types of devices on a single substrate without sacrificing

performance. We also developed all of the processing technology necessary to make monolithic A/Ds on dual-heterostructure wafers.

In Phase II, we invented a new circuit for the RTD-based digitizer in the A/D converter, which included subcircuits for sampling the analog input and latching the digital output. This sampling and latching feature was driven by an external clock, allowing the RTD-based A/D to operate like conventional A/Ds. Based on the new circuit, we designed and layed out masks for making 1-, 3- and 4-bit A/D's along with an extensive process control monitor. We processed several wafers of A/D's using both optical and e-beam written gates. We performed high speed testing on the A/Ds using on-wafer probing at clock rates as high as 2.3 GHz with analog input signals as fast as 0.54 GHz. We believe that this performance could be improved by further shrinking the MODFET gate length and refining our on-wafer testing techniques .

In Phase III, we designed a new mask set for 5-bit and 6-bit A/Ds. Based on what we learned from the 3-bit A/D's, we made several improvements in the design and layout of the circuit. The mask included circuits for 1-bit, 3-bit, 5-bit, and 6-bit A/Ds along with a process control monitor. We made several complete runs of A/Ds with the new mask set. We tested 1-bit, 3-bit, and 5-bit A/Ds and demonstrated their functionality.

We identified both internal DoD and AlliedSignal Aerospace applications for high-speed, low resolution A/D converters. We also developed a plan for manufacturing our A/D converter, and confirmed that the dual-heterostructure wafers, RTDs, and MODFETs (or HBTs) can be processed on a conventional InP pilot production line. Based on our experience and input from several DoD

organizations, we developed recommendations for future technology developments needed to transition these A/D converters to real systems applications.

In summary, we met our objective for this program, to demonstrate the feasibility of a GHz sampling rate RTD-based A/D converter. We developed several innovative designs which took advantage of the RTD transfer characteristic as a basis for A/D conversion. We identified several DoD programs as possible insertion candidates for these devices, and determined that InP pilot lines are in place which can fabricate our A/D converter. While the fundamental device performance and circuit design issues are now well-characterized, further development will be required to move this technology to the prototype stage.

Of all the approaches for high-speed A/D's that have been proposed by ourselves and others, the RTD-based approach offers the best opportunity to achieve sampling rates of 10 GS/s or better at levels of power consumption acceptable to the typical user.

Participants in the Program

In addition to the staff at AlliedSignal MTC, other participants in the program were:

1. Dr. Hung-Chang (Jimmy)Lin - University of Maryland

   -Major sub-contractor

   -circuit design/simulation, high-speed testing

   -three full-time grad students

2. E-Beam Lithography

   Microelectronics Research Laboratory (NSA), Columbia, Md

   Solid State Electronics Lab - University of Michigan

   Nanofabrication Facility - Cornell University

3. Dr. Chia-Hung Yang - University of Maryland

   Modeling Resonant-Tunneling Diodes

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1.0 Introduction

This is the final report and the last deliverable of the ultra-high-speed analog-to-digital (A/D) converter program based on resonant tunneling diodes (RTD). The principle objective for this program was to demonstrate the feasibility of using RTDs in an A/D converter to dramatically improve its speed, lower circuit complexity, and reduce power consumption We invented, designed, simulated, fabricated and tested 1-bit to 6-bit A/Ds. A description of the program, its objectives, approach, and accomplishments is presented below.

1.1 Technical Objectives:

The overall objective of this program was to demonstrate 3- and 6-bit analog-to-digital (A/D) converters with effective sampling rates up to 10 and 4 GHz, respectively, while achieving a size and power consumption that was an order of magnitude less than conventional flash A/D converters operating at comparable speeds. Our A/D converter is one of the first practical applications of the emerging technology of circuits based on resonant-tunneling devices. We divided the program into eight major tasks with subgoals for each task. These tasks were to:

1. Develop the technology for monolithically integrating two high-quality heterostructures, one for multi-well RTDs and one for MODFETs.
2. Demonstrate that all of the components needed for the A/D - RTDs, MODFETs, Schottky diodes, voltage-divider resistors - could be successfully made on an integrated heterostructure.

3. Design a 3-bit A/D with an effective sampling rate of 10 GHz based on the components demonstrated in the second subgoal.
4. Establish a technology for testing the performance for the A/D converter.
5. Process monolithic 3-bit A/D converters which met the performance goals.
6. Design a 6-bit A/D converter with an effective sampling rate of 4 GHz based on the components demonstrated in the second subgoal.
7. Process a monolithic 5-6 bit A/D converter which met the performance goals.
8. Develop a technology insertion plan, including a manufacturing plan, and identify potential system applications for this technology within the DoD community.

1.2 Approach

Our approach was to use a new electronic device, the multi-well resonant-tunneling diode, in a novel A/D circuit invented several years ago by Arbel and Kurz (Ref. 1). A key element in the Arbel and Kurz approach is a rather complex circuit to generate a saw-tooth current-voltage characteristic that is then used for A/D conversion. Our multi-well RTD generates this I-V characteristic in a single small device, greatly simplifying the circuit complexity and reducing power consumption. We achieved high speed operation by using MBE-grown GaInAs/AlInAs heterostructures for the RTDs, MODFETs, and Schottky diodes used in the circuit. This InP-based technology has produced some of the fastest semiconductor devices demonstrated to date. We used selective epitaxy to monolithically integrate on an InP substrate the two heterostructures needed by the circuit. We interacted with potential users of high-speed A/D's within the DoD community to insure that our work was compatible with their future needs.

1.3 Summary of Accomplishments:

The program met its objective to significantly advance in the technology of high speed A/D converters. Several problems were identified and solutions were incorporated. Over the life of the program we:

- Invented two novel architectures for A/D's based on RTDs
- Developed a process for fabricating hysteresis-free RTDs
- Developed a process for making dual-heterostructures on SI-InP substrates.
- Developed a process for fabricating 1-bit to 6-bit A/D converters.
- Developed advanced state-of-the-art on-wafer testing at GHz clock rates.
- Demonstrated working integrated circuits of 1-bit to 5-bit A/Ds, with sampling rates up to 2 GS/sec for 3-bit A/Ds.
- Demonstrated the simulation of complex circuits containing RTDs using SPICE.
- Developed a technology insertion plan

Section 2 presents details of technology development, including progress on the development of monolithic heterostructures and the optimization of component performance. Design, simulation, fabrication, and testing of the 3-bit A/D is detailed in Section 3.0. In Section 4.0, the design, fabrication and testing of the 5-bit and 6-bit A/Ds are described. Section 5.0 addresses technology insertion issues. Finally, Sections 6.0 and 7.0 summarizes our conclusions and outlines future work.

2.0 Technology Development

The goal during this phase of the program was to 1) develop the technology for growing both RTDs and MODFETs on the same InP wafer so that a totally monolithic circuit can be processed, and 2) develop components needed for the A/D converter: RTDs, MODFETs, Schottky diodes, and resistors.

2.1 Wafer Qualification

The quality of InP wafers varies greatly from manufacturer to manufacturer and even from boule to boule from the same manufacturer. Therefore, it was important to carefully qualify every boule of InP wafers. Our experience ha been that we rejected as much as 50% of the boule we received (various vendors), usually for high etch-pit density or for a large drop in resistivity after high temperature annealing.

All of the wafers used for this program were from Crystacomm, as specified in the contract. Three wafers from each boule (top, middle, and bottom) were evaluated for etch-pit density and resistivity and for the effect of annealing on these properties. Only wafers exhibiting etch-pit densities of less than $3X10^4$ cm^{-2} and resistivities (both before and after annealing) greater than 10^7 ohm-cm were accepted.

2.2. Monolithic dual-heterostructure development.

The goal of this task was to develop the technology necessary to monolithically integrate GaInAs/AlInAs MODFETs and GaInAs/AlInAs RTDs on an InP substrate. The MODFETs and RTDs made on this dual-heterostructure wafers must perform as

well as the same devices made separately on conventional single-heterostructure wafers. There are two techniques for integrating the RTD and MODFET heterostructures: 1) selective epitaxy, and 2) vertical integration. We opted to use selective epitaxy rather than vertical integration to integrate the RTDs and MODFETs due to the difficulty of etching off the top device layer completely without etching into the bottom one when processing circuits on vertically integrated substrates. This problem could be solved by growing a thin layer of InP as an etch stop between two heterostructures, but this approach would increase growth complexity . Even then, due to the non-planarity of the surface after removing the top device layer, processing of the circuit would be more difficult, and step coverage of metals could be a problem. Selective epitaxy involves two independent growth runs on selected areas of the wafer, one for each heterostructure, and it results in a planar final wafer surface. The issues addressed during the program were:

1. How to design the first heterostructure to withstand the growth temperature of the second heterostructure.
2. How to minimize the time at elevated temperatures during the second heterostructure growth.

2.2.1 Annealing of the Heterostructures

Prior to the start of the contract we annealed individual RTD and MODFET heterostructures to determine their stability at high temperatures. The MODFET structure shown in Figure 2.1 was annealed from 400-750 °C in a RTA for 5 sec and at 550 °C for 1 hour in a conventional furnace. Plasma-enhanced SiO_2 films deposited at 250 °C were used as cap layers during high temperature annealing. Room temperature Hall mobilities (μ) and sheet carrier concentration (N_s) were measured for

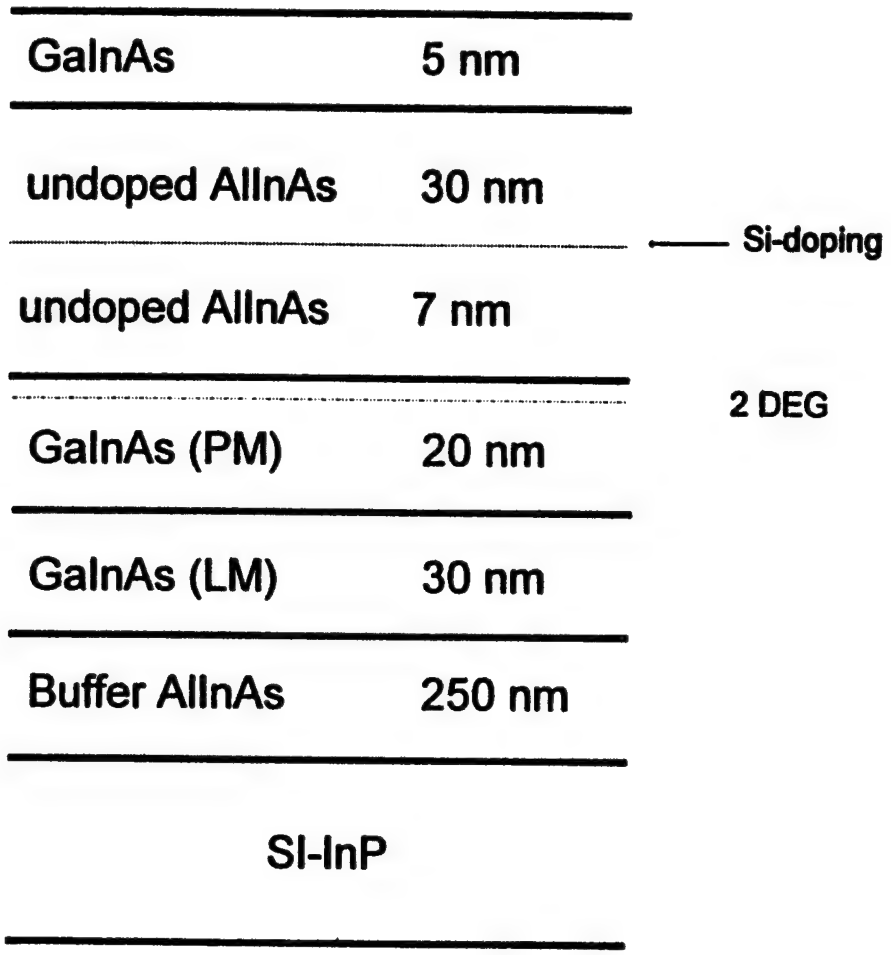


Fig. 2.1 Pseudomorphic $Ga_{.4}In_{.6}As$/AlInAs MODFET used for high temperature annealing

each sample. Figure 2.2 shows that the MODFET structure suffered a drastic reduction in N_s and μ after a RTA anneal at 600 °C. These effects may be due to: 1) diffusion of Si into the spacer layer, 2) diffusion of Ga through SiO_2, or 3) degradation of the pseudomorphic GaInAs/AlInAs interface. Samples annealed in the furnace at 550 °C suffered a similar reduction in mobility and carrier concentration. From these results, it was obvious that the pseudomorphic MODFET structure will degrade if the second growth temperature is above 550 °C.

GaInAs/AlInAs lattice-matched RTD structures, shown in Figure 2.3, with varying spacer layer thickness from 10-40 nm were used to assess the stability of these devices. The structures were capped with SiO_2 and annealed between 500 and 900 °C in the RTA for 5-sec and at 700 °C for 20 min in the furnace. After etching-off the SiO_2 mask, devices were fabricated. The peak-to-valley ratios (PVR) of lattice-matched RTDs with different spacers after high temperature annealing are shown in Figure 2.4. We concluded that the lattice-matched GaInAs/AlInAs RTDs are stable up to 900 °C for 5-sec. The I-V characteristics of the RTD before and after anneal at 700 °C for 20 minutes in the furnace showed minimum change indicating no detectable degradation of the heterostructure.

2.2.2 Integration of RTDs and MODFETs

We used three MBE growth sequences to integrate RTDs with MODFETs. Since the RTD heterostructure is normally thicker than that of the MODFET, for all the growth sequences the thickness of the buffer layer of the MODFET was increased to give a planar surface. All the GaInAs/AlInAs MODFETs and RTD structures were grown by MBE at a substrate temperature of 525 °C. In the first sequence (1) shown in Figure 2.5, the MODFET structure was grown on the entire InP substrate and a SiO_2 mask was

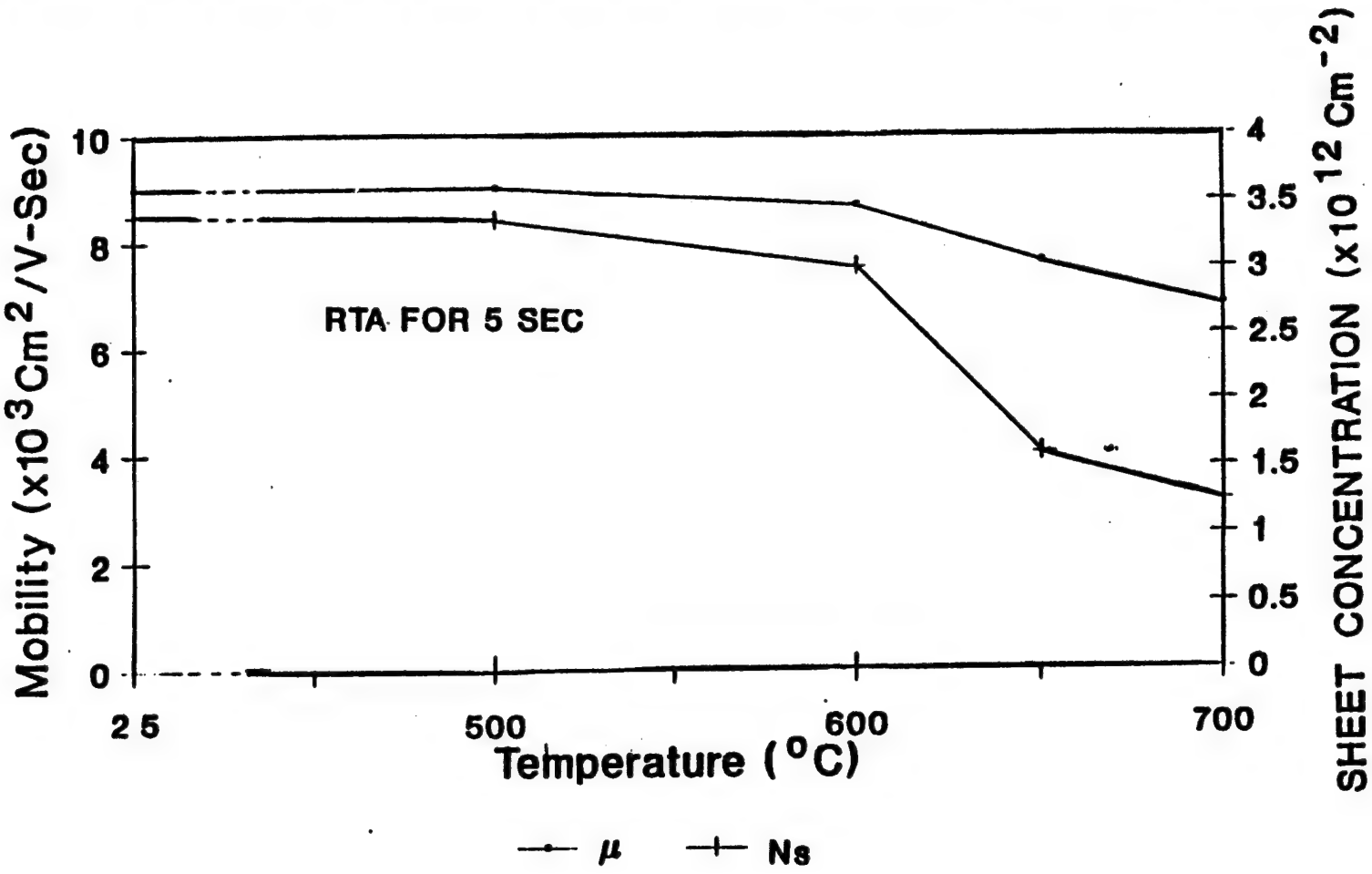


Fig. 2.2 Mobility and concentration versus annealing temperature for a planar-doped InGaAs/InGaAs/InAlAs HEMT

n+ InGaAs	200 nm
undoped InGaAs	10-40 nm
undoped InAlAs	6 nm
undoped InGaAs	6 nm
undoped InAlAs	6 nm
undoped InGaAs	10-40 nm
n+ InGaAs	400 nm
S-InP	

Fig. 2.3 This double barrier resonant tunneling structure was used for high temperature annealing.

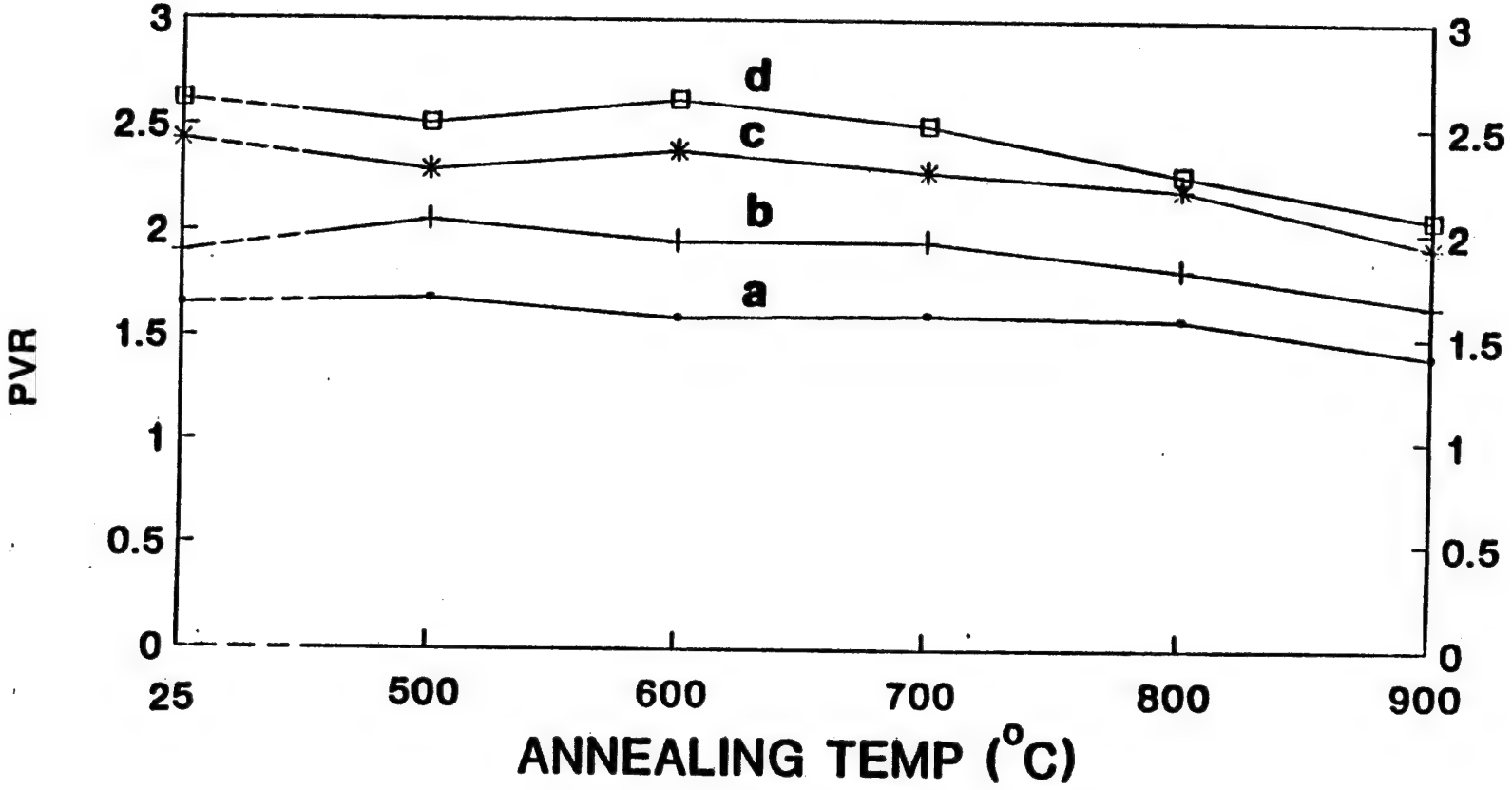
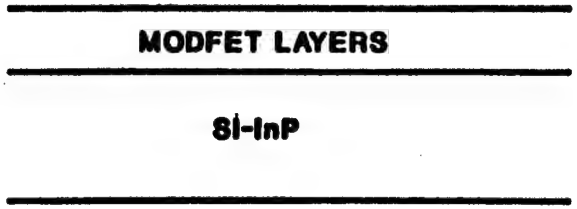
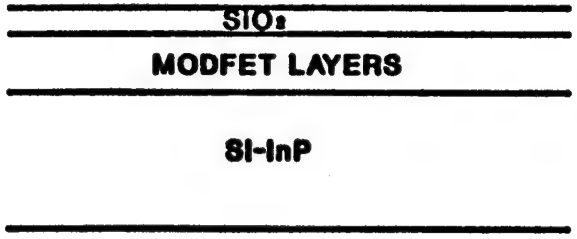


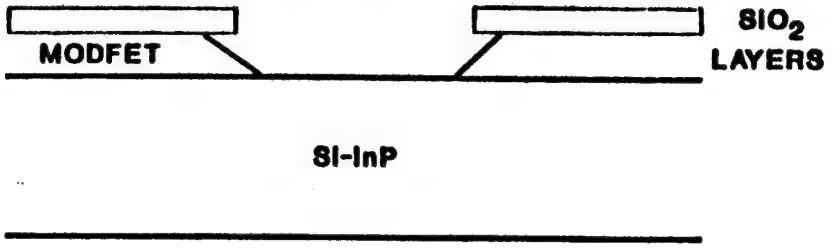
Fig. 2.4 The variations of peak-to-valley ratio of RTDs with annealing temperature. Spacer thicknesses: (a) 10 nm (b) 20 nm (c) 30 nm and (d) 40nm.



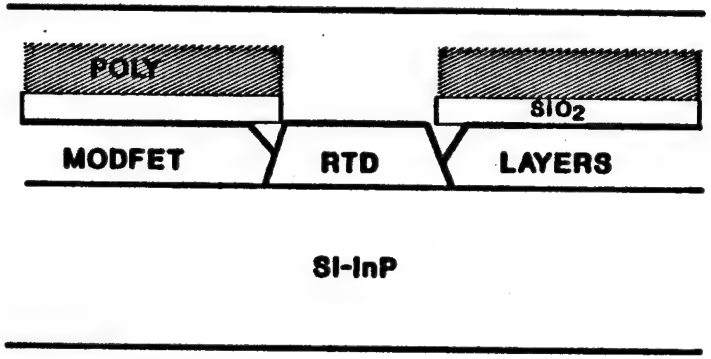
(a) GROW InGaAs/InAlAs MODFET STRUCTURE



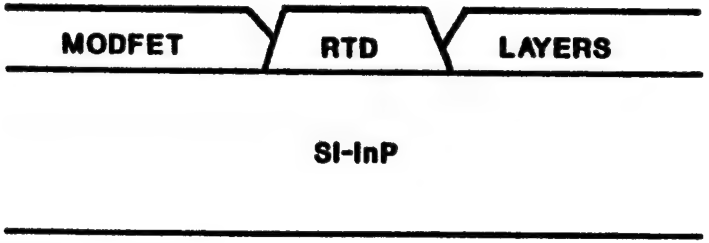
(b) DEPOSIT SiO_2



(c) ETCH SiO_2 AND MODFET LAYERS



(d) GROW RTD STRUCTURE



(e) ETCH POLY AND SiO_2

Fig. 2.5 This selective-epi process degraded the MODFET structure (Sequence 1)

deposited in an ECR - CVD system. In selected areas both the mask and MODFET layers were wet etched. Next, the InP substrate was lightly etched and the RTD layers were grown, single crystal on the InP substrate and polycrystalline on the SiO_2 mask. Finally, the poly-heterostructure and SiO_2 layers were selectively removed via wet etching. Table 2.1 shows the degradation of μ and Ns after the MODFET layers were subjected to the growth temperature of the RTD structure. Figure 2.6 shows the low drain current measured for the MODFET fabricated on the dual-heterostructure grown on SI-InP.

In order to overcome the degradation of the MODFET, we changed to growth sequence (II) as shown in Figure 2.7. We found that no degradation of μ or N_s occurred when the RTD structures were grown first. The I-V characteristics of the MODFET were similar to those obtained from devices fabricated on the structure directly grown on SI-InP substrate. As we expected, no changes in the I-V characteristics of the GaInAs/AlInAs RTDs were observed because of this structure's higher stability than that of the MODFET (2.2.1). Even though the process is simple, the etching step before the growth of the MODFET structure often leads to non-reproducibility in the process. Therefore, we modified the process to our growth sequence III, shown in Figure 2.8, as follows: 1) deposit an SiO_2 film on the InP substrate, pattern and etch a window in the SiO_2, and grow the RTD structure, 2) deposit a second layer of SiO_2 over the RTD heterostructure, 3) selectively etch through the second SiO_2 mask, poly-heterostructure, and first SiO_2 layer revealing the InP substrate 4) grow the GaInAs/AlInAs MODFET structure and 5) remove the poly-heterostructure and SiO_2 over the RTD, leaving behind a planar surface.

Table 2.1. Mobility and sheet concentration of a GaInAs/AlInAs MODFET for various growth conditions.

GROWTH SEQUENCE	MOBILITY cm^2 /V-Sec	Sheet Concentration $X10^{12}$ cm^{-2}
MODFET on SI-InP	11200	1.6
MODFET followed by RTD	9200	0.45
RTD followed by MODFET	11650	1.6

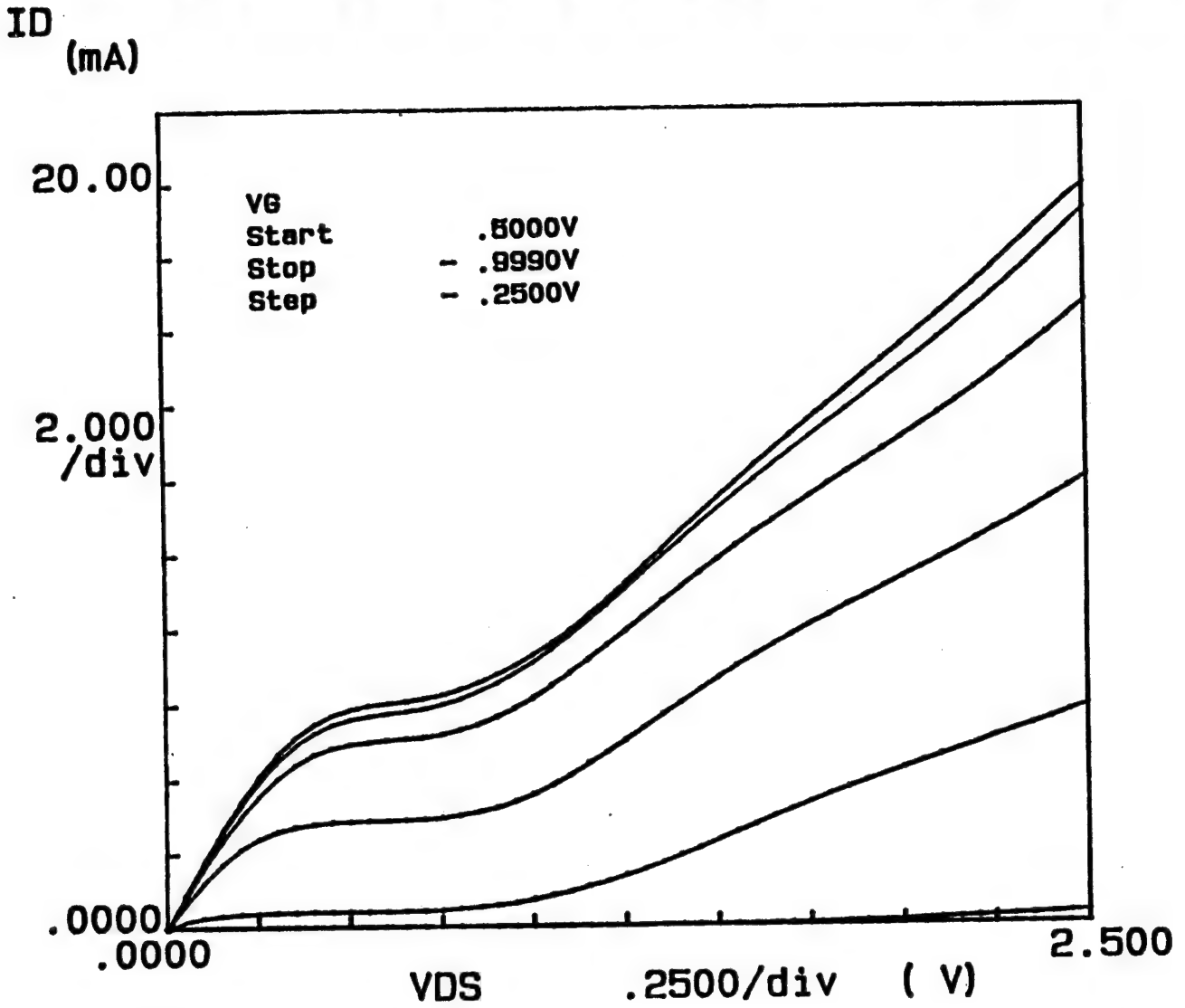


Fig 2.6. IV-characteristics of the GaInAs/AlInAs MODFETs fabricated using heterostructure grown with sequence I. Low Idss indicates degradation of μ and Ns during the growth of the RTD.

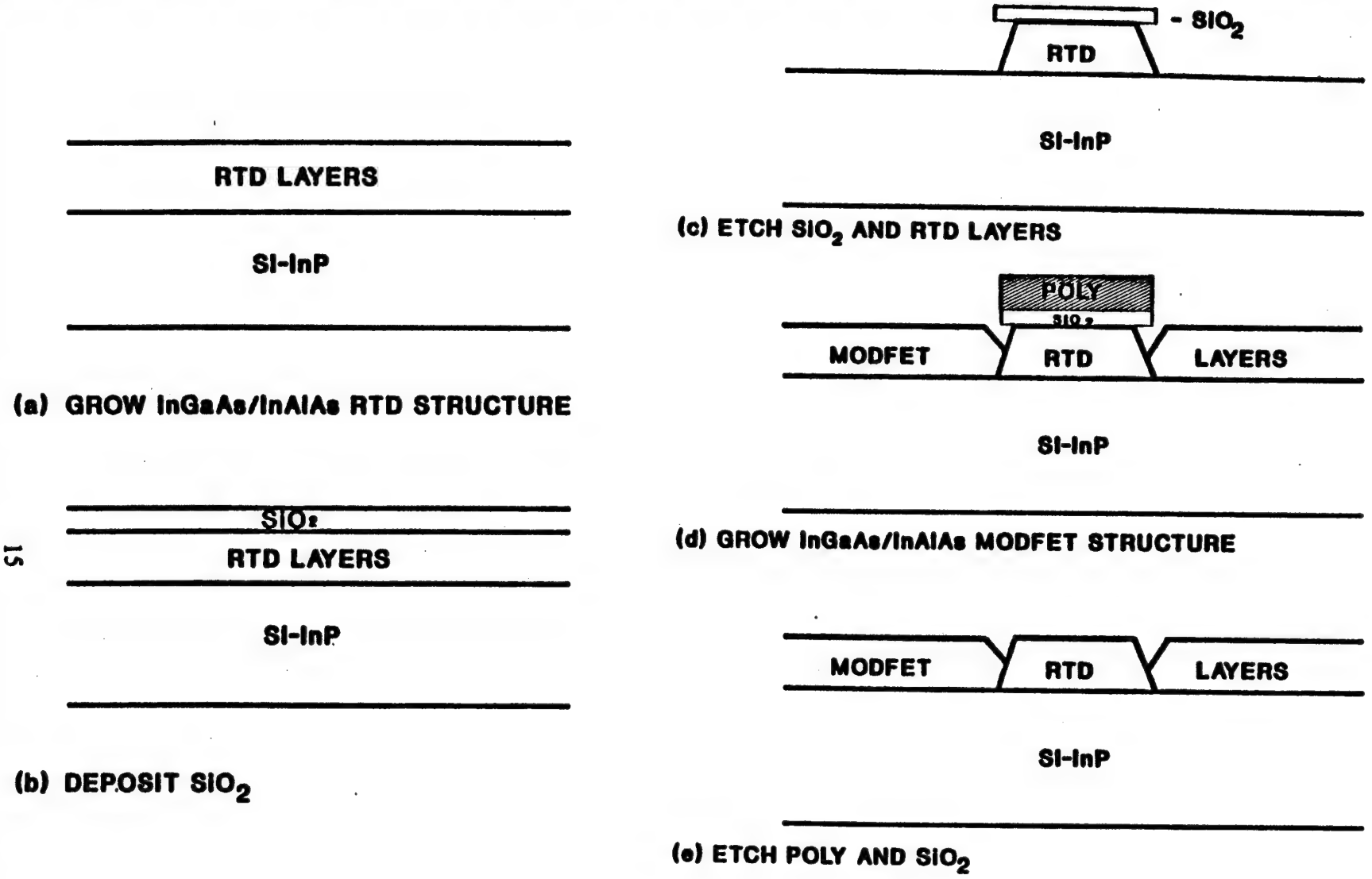
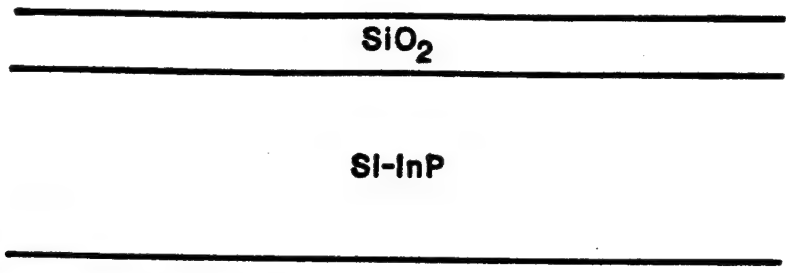
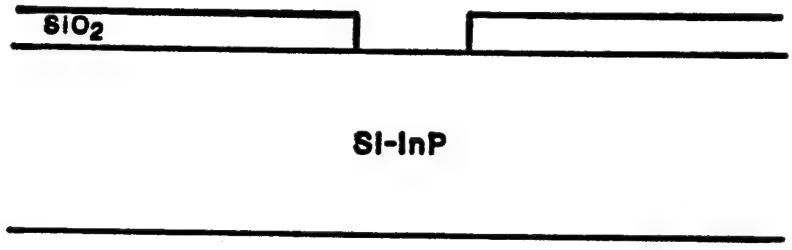


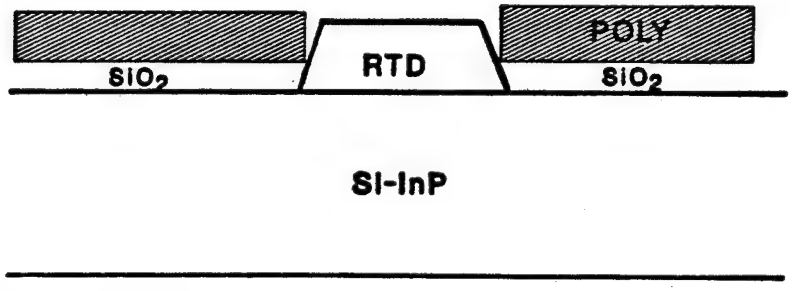
Fig. 2.7 Both heterostructures survived this selective-epi process without degradation, however; reproducibility was a problem. (Sequence II)



(a) DEPOSIT SiO_2 (MASK-1)

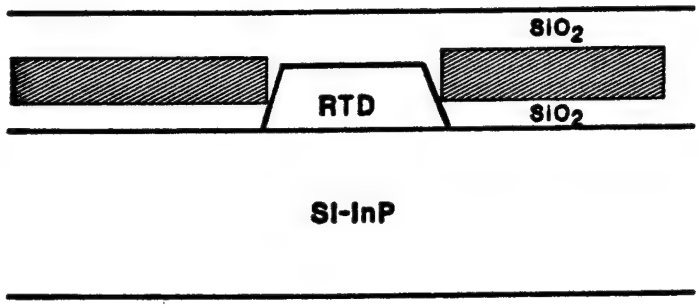


(b) ETCH SiO_2

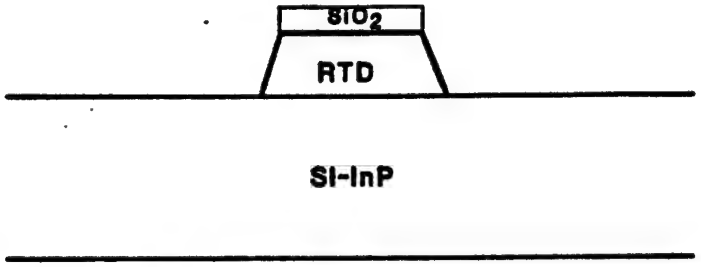


(c) GROW RTD STRUCTURE

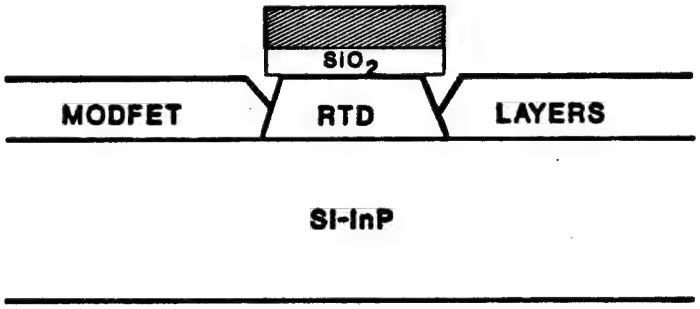
Fig. 2.8 This selective-epi process was used for monolithically integrating the two different heterostructure for the RTDs & MODFETs on a single wafer. This process gave us good reproducible results. (Sequence III)



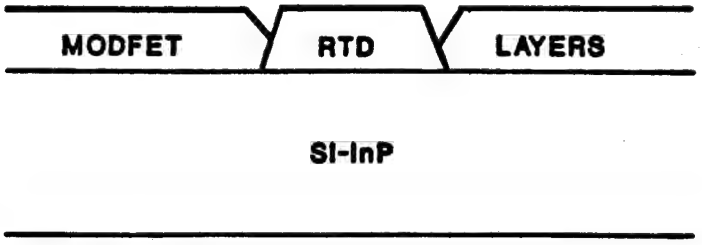
(d) DEPOSIT - SiO_2 (MASK -2)



(e) ETCH MASK-1, POLY AND MASK-2



(f) GROW MODFET LAYERS



(g) ETCH POLY AND SiO_2

Fig. 2.8 Sequence III (continued)

In this process, the InP surface was protected with SiO_2 during the growth of the RTD. After the growth of the RTD layers, the SiO_2 was easily removed leaving a smooth surface for growing the MODFET structures. Figure 2.9 shows a selectively grown island of RTD heterostructure on an InP wafer. Even though this approach involves an additional SiO_2 masking step good reproducibility with smooth surface morphology was obtained. Both the RTDs and the MODFETs on the dual-heterostructure wafers gave the same performance as identical devices we made on separate single heterostructure wafers. Figures 2.10 and 2.11 show the I-V characteristics of MODFETs fabricated on a single heterostructure wafer and dual-heterostructure wafers, respectively.

During the optimization of the RTD heterostructure, we discovered that an InAs sub-well is a must for eliminating hysteresis effects (Section 2.3). Since the final RTD structure was pseudormorphic, we evaluated the thermal stability of these layers at the growth temperature of the MODFET layers. The pseudomorphic RTD structures were annealed from 500-700 °C in a furnace for 30-45 minutes. Devices were fabricated on all the annealed as well as the unannealed samples. The effect of post growth annealing for the InAs subwell and AlAs barrier RTD is given in Table 2.2. We found that: 1) annealing improves the PVR up to 550 °C, but then it decreases at higher temperature, 2) the peak current as well as the valley current increases with temperature and 3) the increase in the PVR can be attributed to strain relaxation, and the reduction in PVR is due to interface degradation. Taking these aspects into consideration, we optimized both the design of the RTD and the growth temperature of the MODFET. The RTD heterostructure was selected to give a lower peak current than the desired value before MODFET growth. The final peak current of the RTD after the growth of the MODFET heterostructure was then within the specification. We routinely

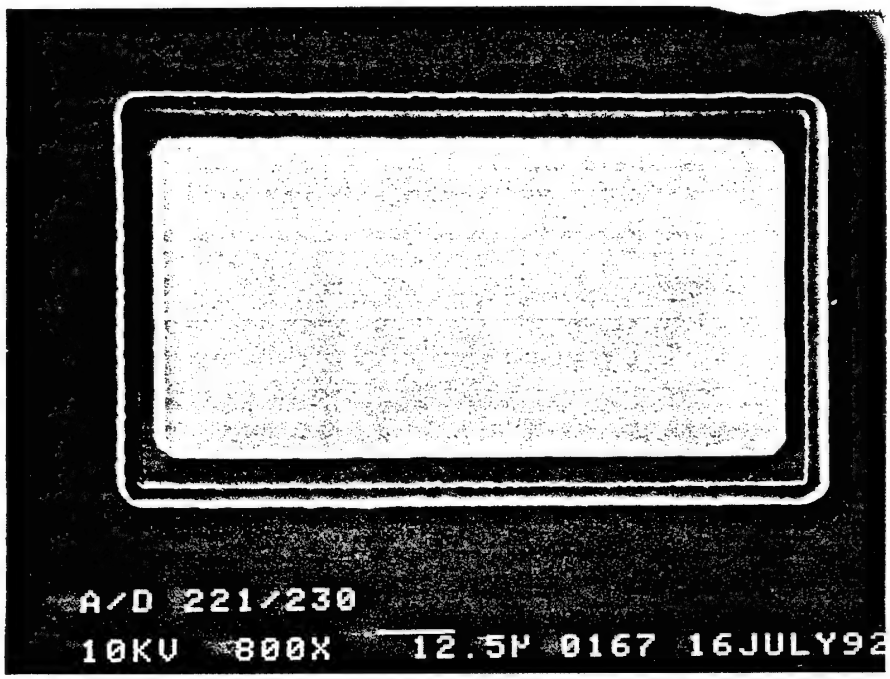


Fig. 2.9 This scanning electron micrograph shows an island of RTD surrounded by MODFET layers.

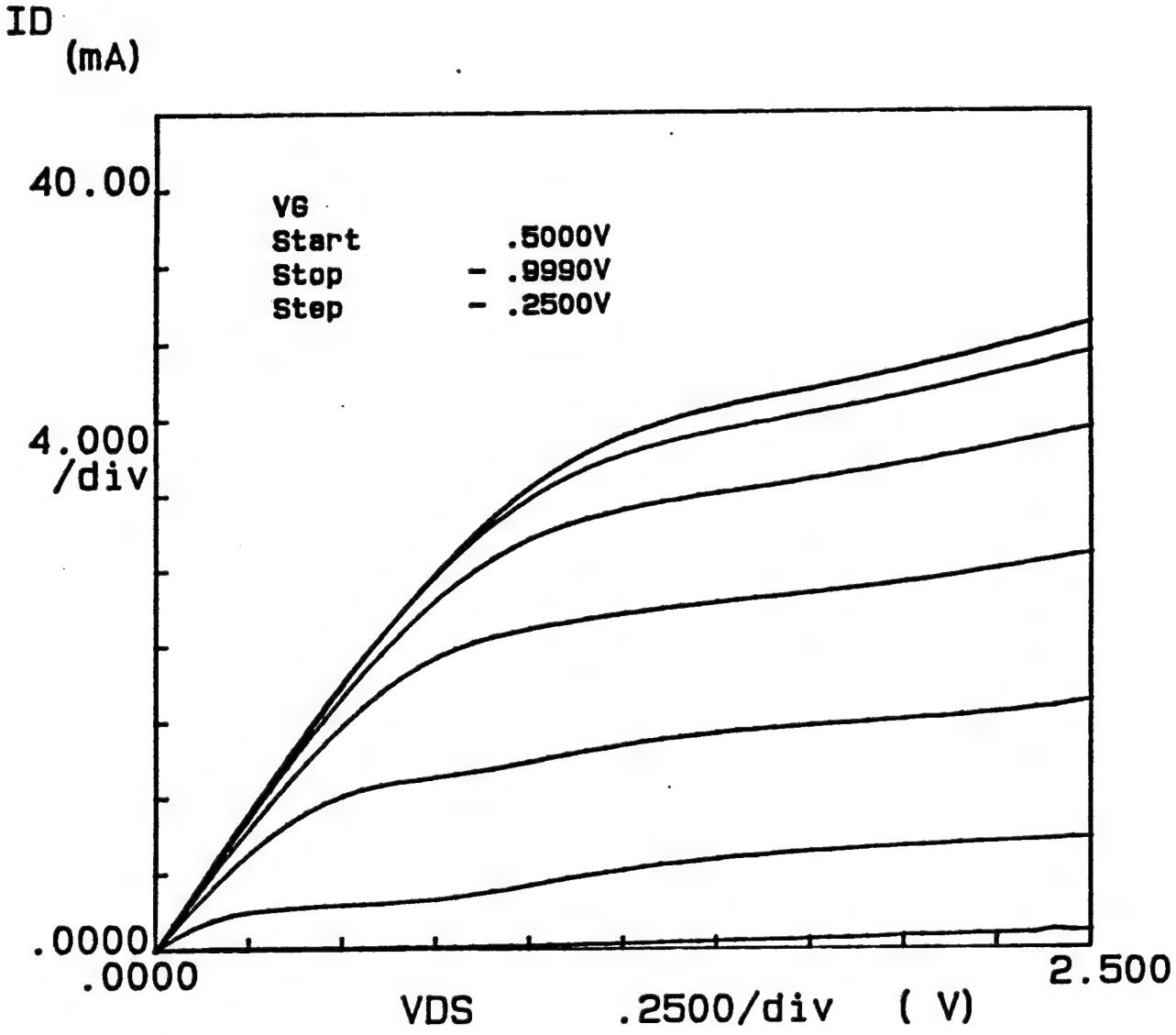


Fig. 2.10 GaInAs/AlInAs MODFET IV-characteristics: single heterostructure grown on SI-InP

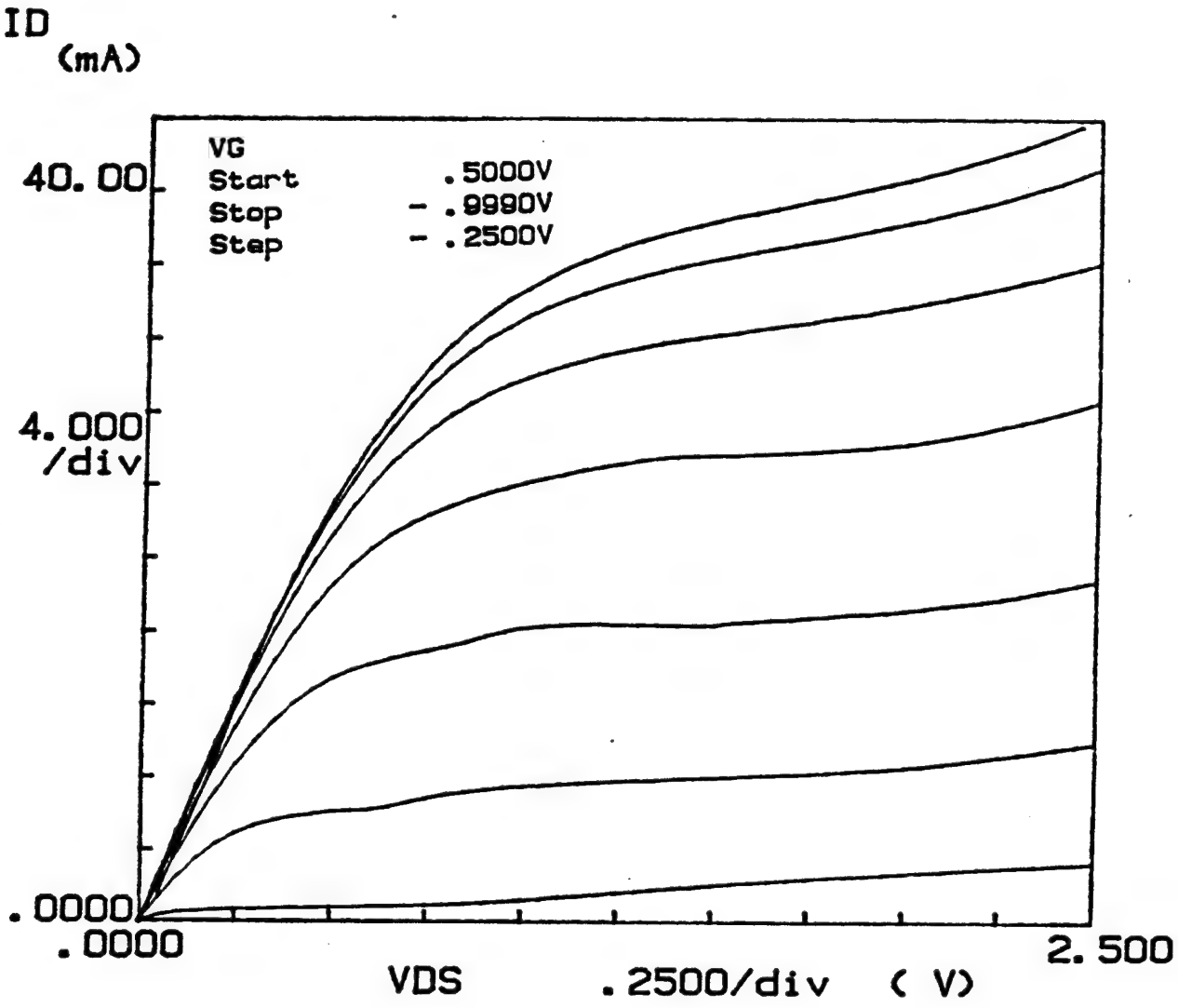


Fig. 2.11 IV-characteristics of GaInAs/AlInAs MODFETs grown with sequence III.

Table 2.2. This table shows the effect of annealing an RTD with an InAs sub-well. The RTD was annealed for 45 minutes in forming gas.

Temperature	PVR
unannealed	1.8
525 °C	2.0
550 °C	2.5
575 °C	1.7

used this process during the contract. We also at times added a layer of undoped AlInAs between the InP substrate and the doped GaInAs bottom contact of the RTD to improve the InP surface morphology after etching. This AlInAs layer would be etched from the substrate before growing the MODFET in the second MBE run.

In summary, we found that:

- The RTD must be grown before the MODFET
  - MODFET performance degrades after exposure to RTD's growth conditions
  - Changes in RTD characteristics due to the growth of the MODFET can be compensated by proper RTD design.
- Careful design of the RTD and MODFET heterostructures result in high-performance devices and a planar surface.
- Planar structures are necessary for high yield, optical gate contact lithography.

2.3 RTD Development

The design of the RTD structure was very critical to the success of the A/D converter program. The objectives for this task were to design and fabricate a multi-peaked RTD with: 1) a high current/capacitance (I/C) ratio, 2) a current density of about 5000A cm^{-2}, 3) a peak-to-valley ratio of at least two, 4) a hysteresis free I-V characteristic, and 5) uniform current peaks and valleys. The speed of the A/D is a strong function of the I/C ratio but it only weakly depends on the PVR, if the PVR $\geq$ 2.0. Therefore, we optimized the structures to have a large I/C ratio at the expense of PVR.

In the original proposed A/D design we required a 4-peak RTD without hysteresis in the I-V characteristics. Prior to the start of the program, we vertically integrated 5-peak RTDs with uniform peak spacings which exhibited hysteresis. Hysteresis complicates the design of the A/D (section 4.1.1) and results in slower sampling rates. For RTDs in series to be free of hysteresis, $R_n > (m-1)R_p$, where R_n and R_p are the device negative and positive differential resistances respectively and m is the number of wells in each RTD. The resolution of the A/D converter is determined by the uniformity of the peak-to-peak voltage and peak-to-valley current of the multi-well RTD I-V characteristic. These values are determined primarily by the thicknesses of the spacer, barrier, and well layers that make up the vertically integrated structure of the multi-well RTD.

In the original RTD-based A/D converter, we proposed using a lattice-matched GaInAs/AlInAs heterostructure for the RTD. Many runs were made to optimize a 4-peaked RTD to satisfy the complex requirement described above. The optimization process involved varying the spacer, barrier, and well widths. The current density was increased by reducing the thickness of the barrier or the well. Decreasing the

thickness of the barrier reduced the PVR and decreasing the thickness of the well increased the PVR. Fortunately, none of these changes greatly affected the capacitance, which permitted us to independently maximize the I/C ratio.

Earlier in the program, we consulted Prof. Yang from the University of Maryland for analytical guidance in the design of the RTD. He showed through analytical modeling that asymmetrical spacers and barriers with little or no spacer on the collector side and a wider barrier on the collector side than on the emitter side should result in the lowest possible hysteresis. Most of these changes were incorporated, and several devices were fabricated, but only a marginal reduction in the hysteresis resulted.

We have seen zero hysteresis in 8 μm diameter RTDs. Hysteresis increases monotonically above 8 μm as the diameter of the RTD increases. This observation supports our hypothesis that the parasitic resistance which causes hysteresis is due to current crowding around perimeter of the RTD; the smaller RTDs have less current crowding per unit perimeter. To further verify this idea, we processed self-aligned RTDs (no heavy doping) to reduce this resistance and found reduced hysteresis. Therefore, we designed and ordered new RTD masks to test the effect of geometry on hysteresis. Figure 2.12 shows the layout of this new RTD mask.

We processed devices to experimentally compare the use of single-well, and 2-well RTDs connected in series to give 4-peaks equivalent to that of a single 4-well RTD. The single well and 2-well RTDs were connected through a common n^+ layer beneath them, leaving top contacts for connection to the circuit. The I-V characteristics of the 2-well RTD connected in series to give 4-peaks exhibited non-uniform characteristics. SIMS analysis of similar heavily doped GaInAs layers indicated that the dopant is

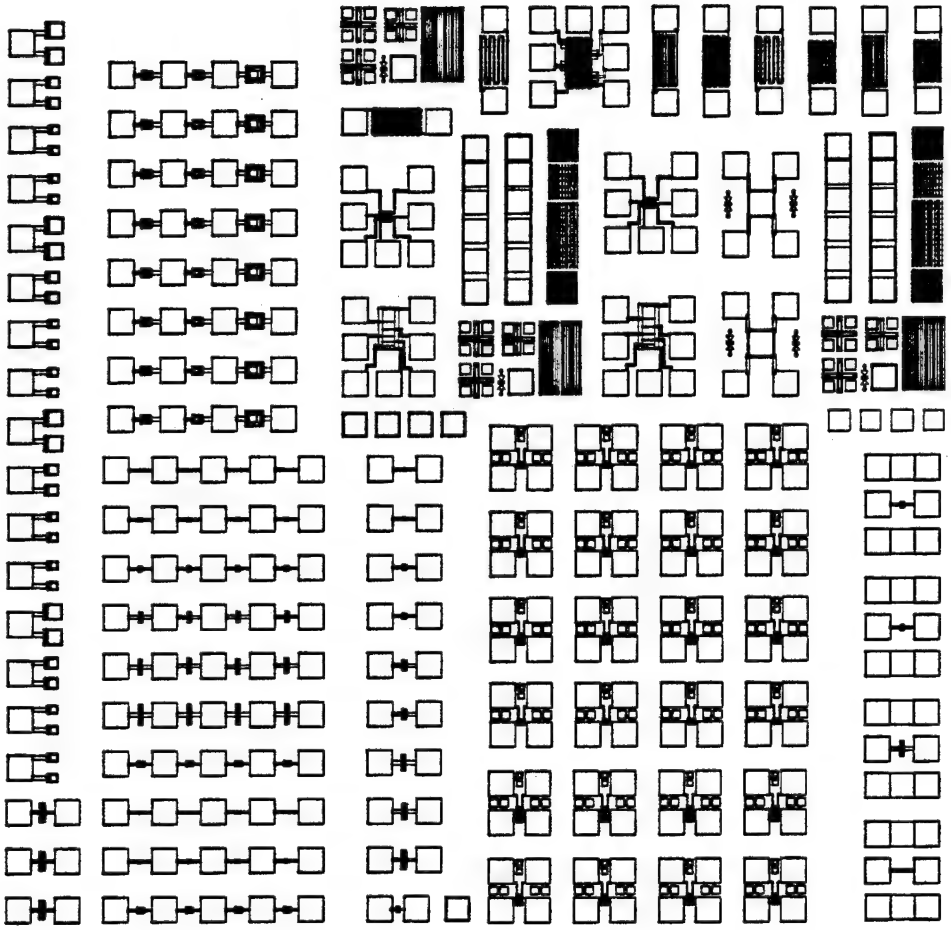


Fig. 2.12 Layout of the RTD mask used to evaluate the effect of geometry on hysteresis.

diffusing into the undoped spacer layer on one side of the RTD, reducing or eliminating the spacers on that side only and creating an asymmetrical spacer. We found that it is easier to achieve uniformity in the peak heights and the peak-to-peak spacing in the I-V characteristics of the single-well RTD connected in series. This also simplified the circuit processing since connecting to the top contact is much easier than connecting to the bottom contact of the 4-well RTD.

The most significant result in the optimization of the RTD was the incorporation of an InAs subwell in the GaInAs well. This resulted in the first 4-peaked, hysteresis free device with uniform peaks in the I-V characteristic. The presence of the subwell caused the level in the well to be pulled down in energy. This had the net effect of lowering the voltage at which the peak current occurred. More importantly though, it increased the net amount of NDR available; in other words, the subwell increased the voltage difference between the peak voltage and valley voltage. Because of the significant increase in the NDR, more devices could be connected in series without hysteresis. The InAs subwell had one drawback - it caused the valley current to increase which resulted in a reduced peak-to-valley ratio of about 2:1. The I-V characteristic shown in Figure 2.13 for this RTD structure illustrates near zero hysteresis, an asymmetric I-V, and a peak-to-valley ratio of about 1.4:1. The voltage span for the 4-peaks is less than 2.0 V. Although the RTD structure is nominally symmetrical, the I-V characteristics are asymmetrical, due to the asymmetry in the roughness of the interface in the MBE-grown structure. This is not a problem since the RTDs only operate in the first quadrant of their I-V characteristics in the A/D circuit. In order to understand this behavior, we fabricated RTDs by growing the layers in the following sequences. 1) AlAs, InAs, GaInAs, AlAs, and 2) AlAs, GaInAs, InAs, AlAs

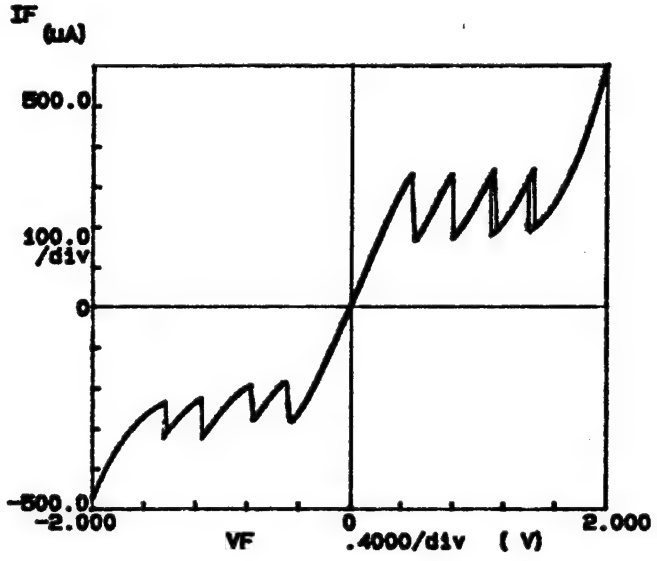


Fig. 2.13 This I-V characteristic for a 4-well RTD containing InAs subwells in the InGaAs wells is very close to what we need for the 4-bit A/D converter

and found negative differential resistance in the first structure. This indicates growth of subwell (InAs) on binary (AlAs) gives good interfaces whereas that of InAs on ternary (GaInAs) results in interface roughness which explains the asymmetrical I-V characteristics. We processed several RTDs by varying the total thickness of the well, the thickness of InAs sub-well relative to GaInAs, and the thickness of the barrier and spacers (thickness composition and doping). Decreasing the thickness of the well increased the negative differential resistance. Increasing the thickness of the InAs subwell (for a given well thickness), decreased the positive differential resistance, but reduced the PVR.

We also fabricated RTDs with 1) ECR-CVD deposited SiO_2 and Si_3N_4 and 2) pyrolitic-CVD deposited SiO_2 and found no change in I-V characteristics for all the dielectric films. After making more than a hundred MBE growth and processing runs to develop the optimum structure for a hysteresis-free, multi-well RTD, we finally selected a structure for use in the next stage of the project. The structure is shown in Fig. 2.14 along with an example of the dc characteristics of a 4-well RTD, which contains 4 of these structures in series. This is the most impressive example of a hysteresis-free, multi-well RTD that we have ever seen, either from our own work or from the published work of others. The peak-to-valley ratio is almost 2:1 and the peak heights and peak-to-peak spacings are very uniform. The slight amount of negative-differential-resistance that can be seen at a voltage just above the voltage of the fourth current peak proves that this device has no dc hysteresis. The I-V characteristics of the 6-single well RTDs connected in series is shown in Fig. 2.15. This same structure can be used for 2- or 3-well RTDs, or we can trade-off some negative-differential-resistance for

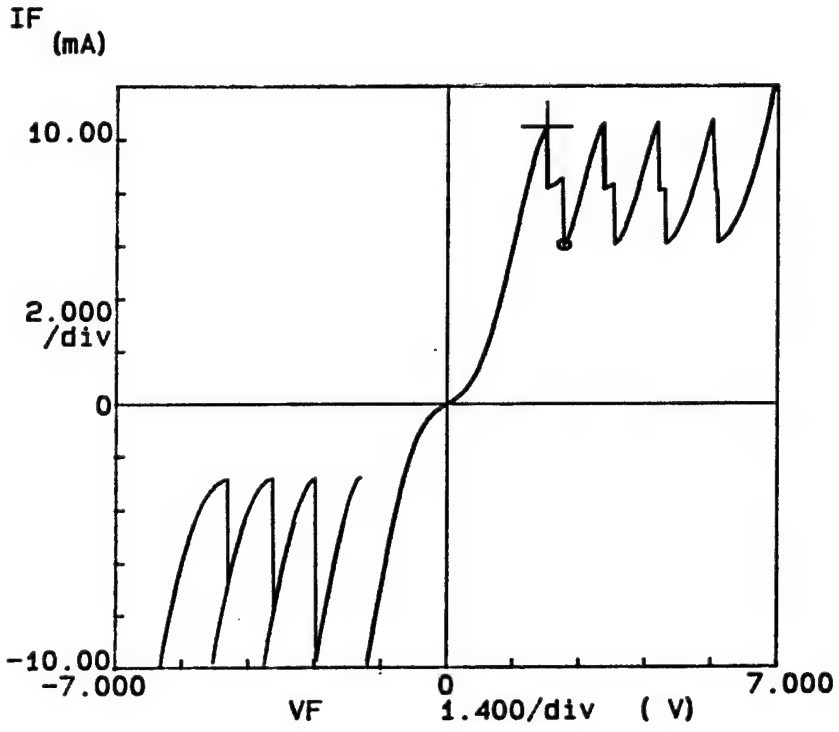


Fig. 2.14(a) The I-V characteristics of a 4-well, hysteresis-free RTD. This is the best example of a hysteresis-free multi-well RTD reported by any lab.

100 nm	N+ GaInAs CONTACT
15 nm	GaInAs SPACER
2.0 nm	AlAs BARRIER
1.4 nm	GaInAs WELL
2.0 nm	InAs SUB-WELL
1.4 nm	GaInAs WELL
2.0 nm	AlAs BARRIER
15 nm	GaInAs SPACER
500 nm	N+ GaInAs CONTACT
SEMI-INSULATING InP SUBSTRATE	

Fig. 2.14(b) Structure of one of four wells that resulted in a hysteresis free RTD.

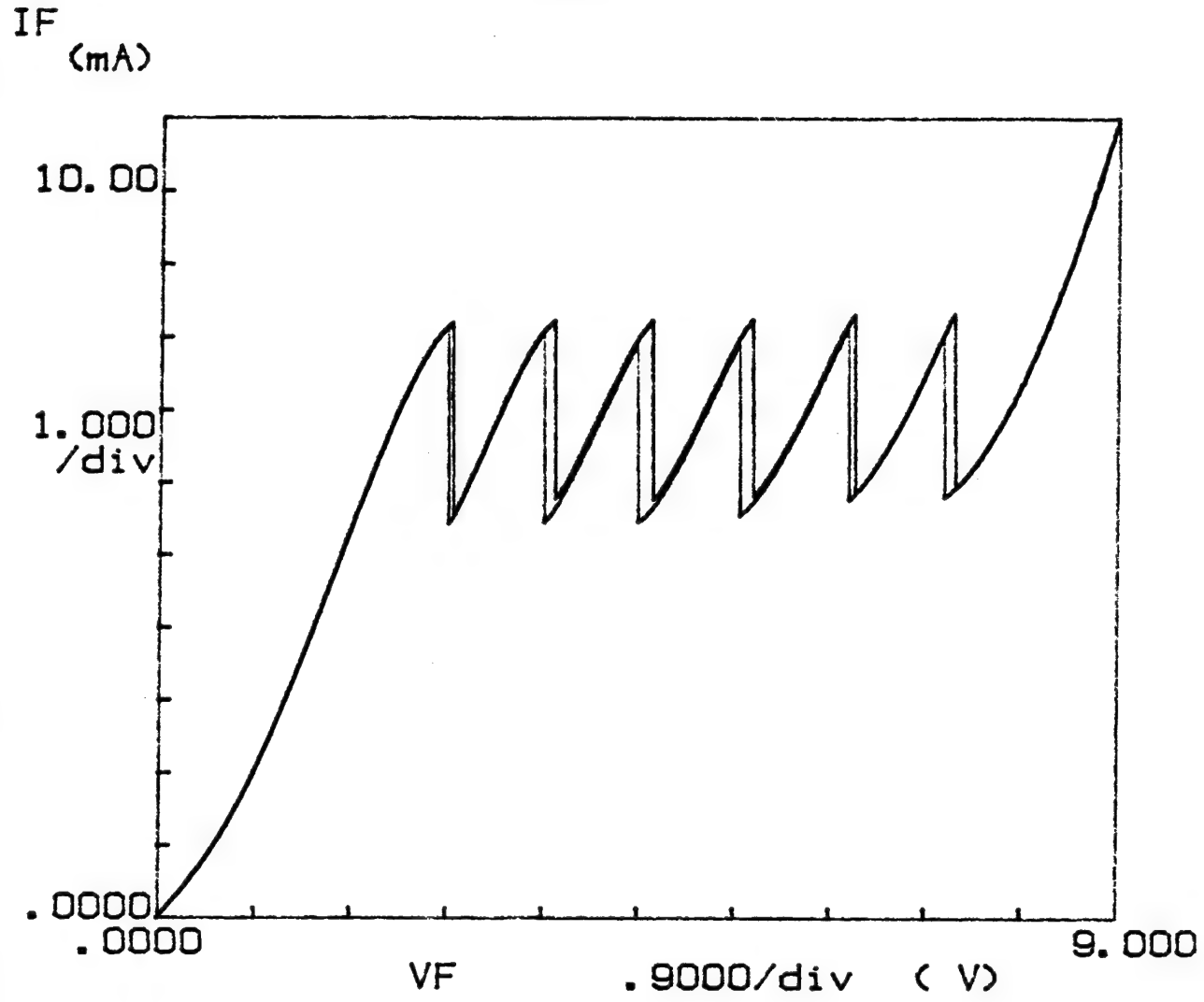


Fig. 2.15 The I-V characteristics of a virtually hysteresis free RTD with six peaks and PVR approaching 2.1.

higher peak-to-valley ratio by slightly decreasing the well width. We have tried growing the entire multi-well RTD as one vertically integrated structure or making single-well structures and connecting them in series. The latter approach gives more uniform peak heights and since the RTDs will take up negligible space on the A/D chip, we plan to connect single-well devices in series. This device represents an important step towards making other RTD-based circuits in addition to A/D converters.

Although we did make hysteresis-free 4-peak and 3-peak RTDs, we had to sacrifice too much in their PVR, and they could not be used in A/D circuits. Since we could not use these devices, we felt that an 8-bit A/D was too ambitious at that time. Therefore, we settled on a 3-bit and 6-bit A/D with concurrence with ARPA/ONR. Since the final design of the A/D (Section 3.1.1) only needed a 2-well RTD, this gave us the larger margin needed in the negative differential resistance.

After completing an extensive variations of parameters study, we selected the structure shown in the Figure 2.14 with the specification shown in Table 2.3. The major conclusions from this study were:

- For m well RTD's in series to be free of hysteresis, $R_n > (m-1) R_p$, where, R_n = negative differential resistance and R_p = Positive differential resistance
- Adding a subwell to the RTD reduces positive differential resistance
- Reducing hysteresis in series RTD's reduced the peak-to-valley ratio
- Accurately reproducing RTD's electrical characteristics is tricky

Table 2.3 Specification for the AlAs/GaInAs-InAs-GaInAs/AlAs RTD

Device Parameter	Target Range
Peak voltage	0.18 - 0.22 V
Peak current density	5-10X10^3 A/cm^2
Peak-to-valley ratio	2 (min)
Peak-to-peak spacing	0.28 V

2.4 GaInAs/AlInAs MODFET Structure

2.4.1 0.5 μm Optical Gates

Figure 2.16 shows the structure of the GaInAs/AlInAs MODFET used in the A/D circuits. The excellent performance of these MODFETs is due to planar doping, a pseudomorphic channel, and a GaAs cap. The GaAs cap eliminates the need to recess the gate and also results in pinning of the Fermi level. This makes the Schottky barrier height and threshold voltage uniform over the wafer and reproducible from run-to-run. Planar doping reduces the gate-to-channel separation, thereby increasing the transconductance of the FET. We have measured maximum available gains up to 15 dB at 26.5 GHz for our 0.5 μm GaInAs/AlInAs MODFET. We optimized the sheet carrier concentration to increase the BV_{ds}. Figure 2.17 shows BV_{ds} as a function of gate voltage for the MODFET. Each measurement is a destructive test, and each value plotted is the average for six FETs. All the FETs tested were from the same wafer.

We also evaluated the effect of passivation on the MODFET using: 1) ECR-plasma deposited SiO_2, 2) ECR-plasma deposited Si_3N_4 and; 3) pyrolitic-CVD deposited SiO_2. The ECR films were deposited at 200 °C and the pyrolitic CVD at 300 °C. The I-V characteristics of MODFETs passivated with these films are shown in Fig. 2.18. Microwave measurements show minimal device performance degradation for devices passivated with ECR-deposited films.

2.4.2 E-beam Written Gates

Simulations of the new circuit done at the University of Maryland showed (see subsection 3.14) that we needed a faster FET than the 0.5 μm gate length

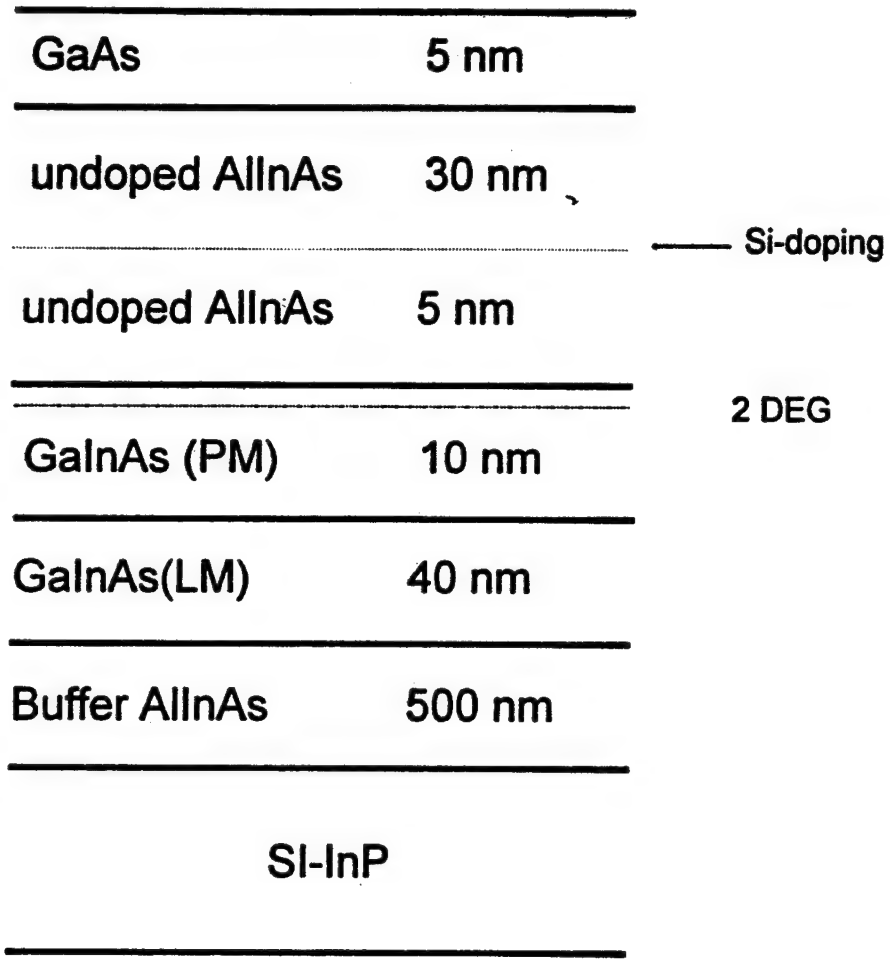


Fig. 2.16. Structure of the pseudomorphic GaInAs/AlInAs MODFET used in the A/D circuits.

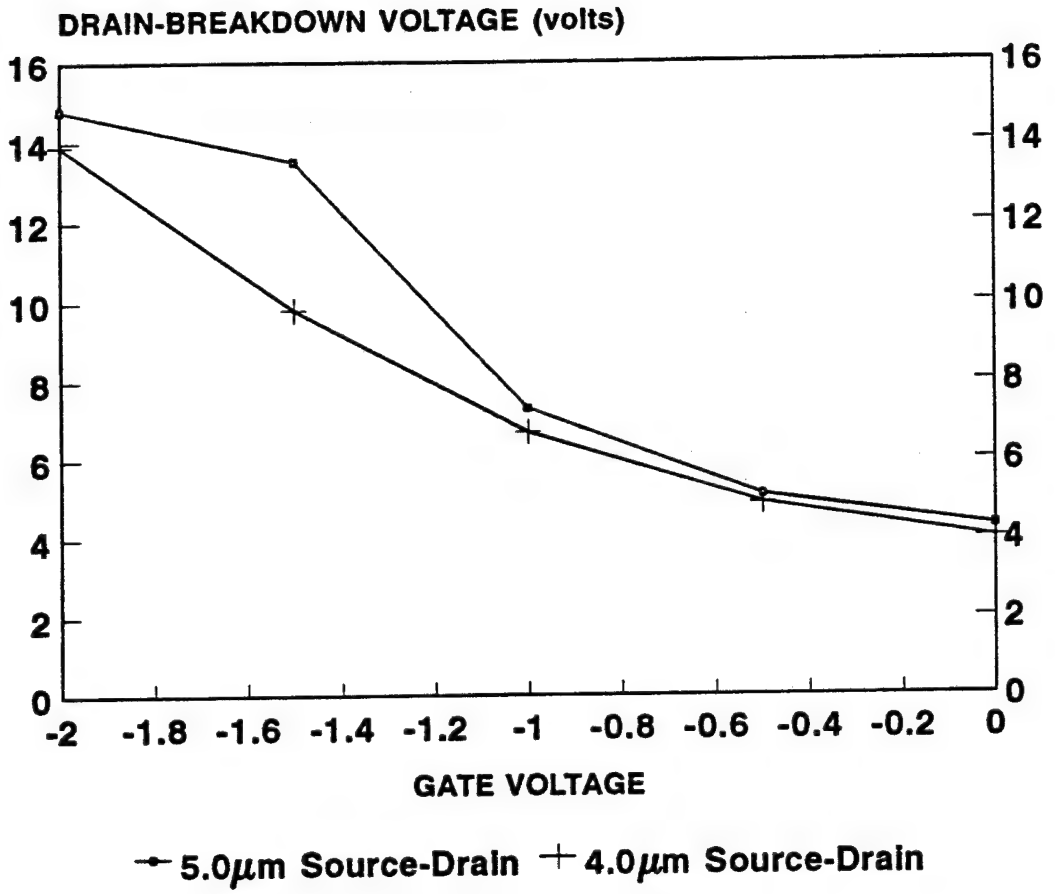
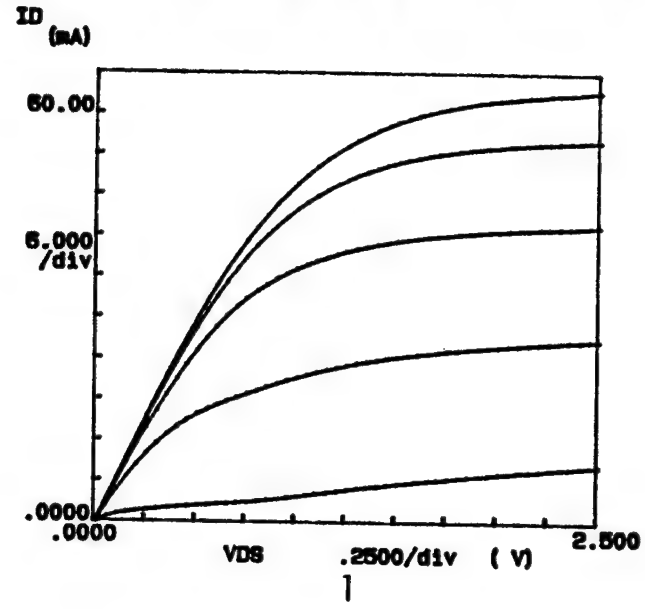
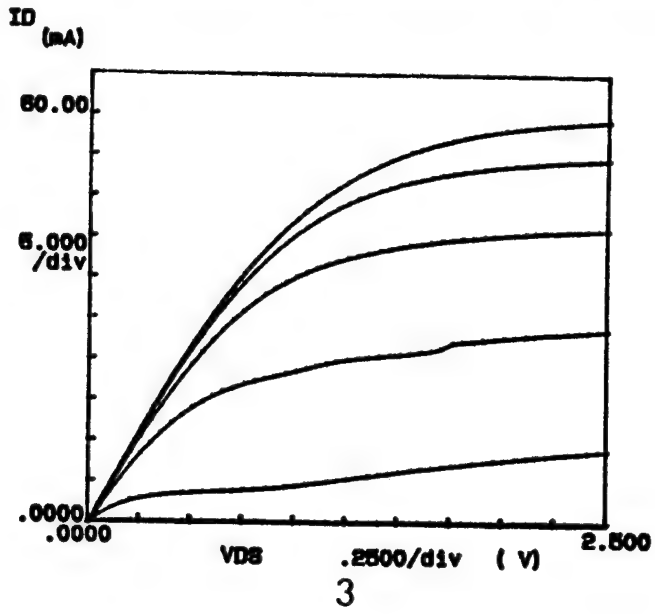


Fig 2.17 This shows high drain-source breakdown voltage of the GaInAs/AlIn MODFET with epbeam written, o.5 μm gates.





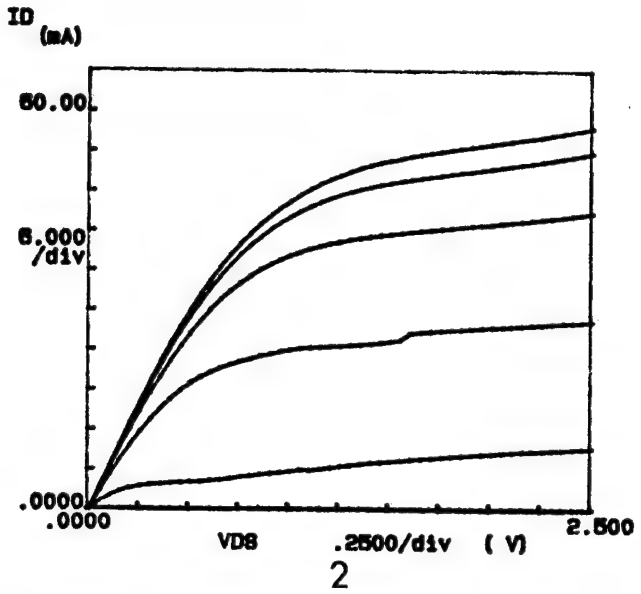
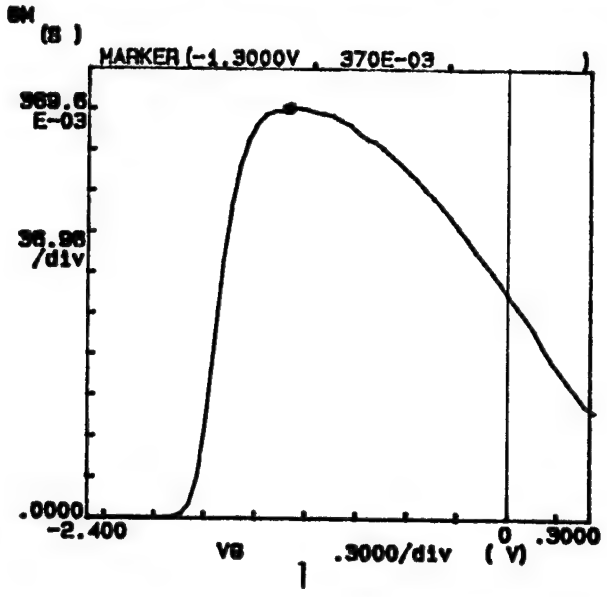
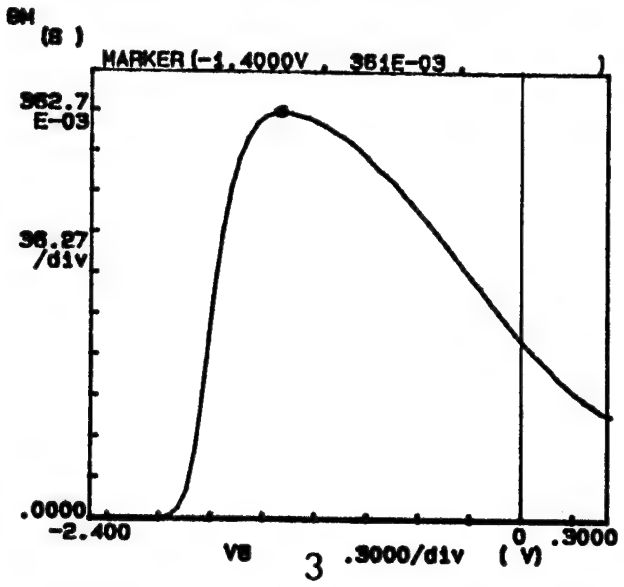


Fig. 2.18 (a) I-V characteristics (1) Pyro SiO_2 (2) ECR-SiO_2 and (3) ECR-Si_3N_4 (start V_g=0.5V, stop V_g = -2.0 V)





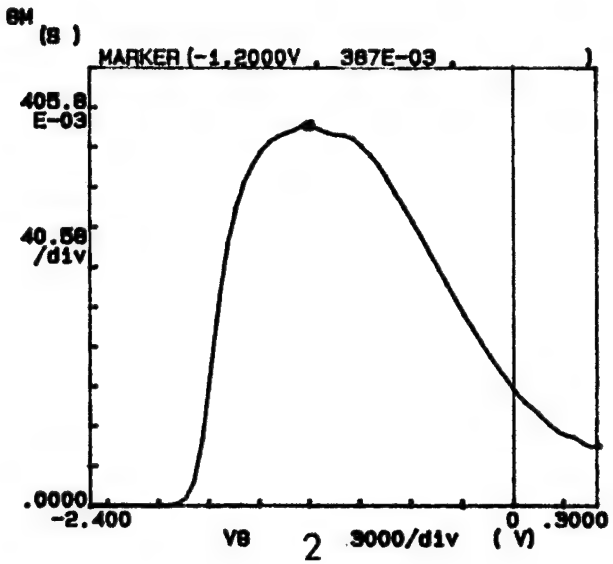


Fig. 2.18(b) Variation of transconductance with gate bias (1) Pyro SiO_2 (2) ECR-SiO_2 and (3) ECR-$Si3N_4$ (V_{ds} = 2.0 V)

GaInAs/AlInAs MODFET proposed in the original proposal. Therefore, we decided to develop 0.25 μm e-beam written gates to meet the 10 GSps sampling rate for the 4-bit A/D converter. As mentioned earlier, the success of the program depended on very good circuit yield, alignment, and dimensional control of the gate level. We have been fabricating 0.5 μm gate length devices using optical lithography since 1987. We also demonstrated that we can control these factors well enough with optical lithography to make the A/D circuits. However, for making the 8-bit, 4 GSps, we need a higher degree of control over the gate length that can be achieved with contact optical lithography , and chose to use direct write e-beam lithography. We worked with the Solid State Electronics Lab at University of Michigan to develop both 0.5 μm and 0.25 μm gate length devices using e-beam lithography.

We processed a few wafers of dual-heterostructure up through the ohmic level and sent them to the U. of Michigan for gate writing. After the gates were written, we deposited and lifted-off TiAu gates. Obviously the yield, alignment, and dimensional control was better than we could do with optical contact lithography. These initial wafers exhibited a higher cut-in voltage for the Schottky diode caused by the "descuming process" used to remove the PMMA resist. Figure 2.19 shows a typical 0.25 μm MODFET with a 4.0 μm source-drain spacing. The larger source-drain spacing and low sheet carrier concentration were chosen to increase BV_{ds} for the FET. We evaluated ECR-Plasma SiO_2 for passivation. These films were deposited at 200 °C using a SiH_4 and N_2O gas mixture. No degradation in FET performance (dc or rf) was observed. We processed several runs of 0.25 μm gate length devices and characterized their microwave performance. From on-wafer measurement of the S-

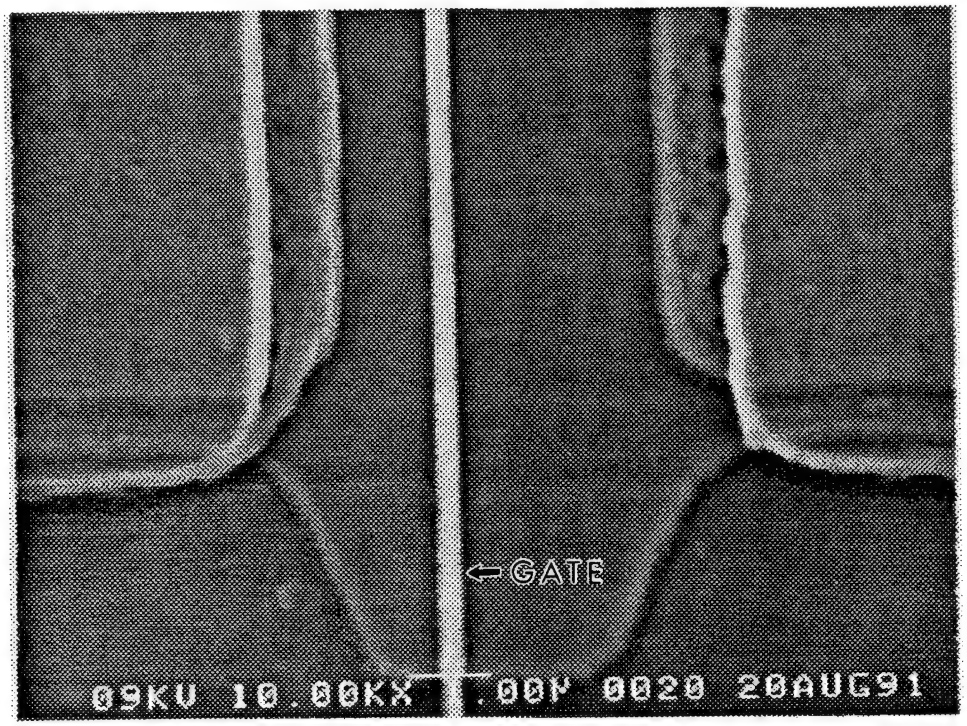


Fig. 2.19 This SEM photo shows the 0.25 μm gate at the edge of the mesa in the GaInAs/AlInAs MODFET. The gate was e-beam written at University of Michigan using our A/D test mask.

parameters, we extrapolated f_T's up to 85 GHz. When corrected for pad capacitance, the f_Ts were about 100 GHz, which was a significant improvement over our previous results with 0.5 μm gates. However, the BV_{ds} (at $V_g = 0$) for these devices was about 3.0 V, less than the desired value.

After completing the development of the GaInAs/AlInAs MODFETs, which included MODFETs with both optical and e-beam written gates and gate lengths ranging from 0.5 μm to less than 0.25 μm, we finally settled on e-beam written 0.5 μm gates for the monolithic A/D circuits. E-beam writing of gates was selected because of its higher yield. The 0.5 μm gate length was selected because of the need for a higher BV_{ds}. Just reducing the gate length to 0.25 μm while keeping the heterostructure and source-drain spacing the same did not significantly improve f_T. However, increasing the channel-current density and reducing the gate-to-channel spacing improved the f_T, but reduced BV_{ds} even further. Table 2.4 shows the final device parameters used in the design of the A/D.

2.5 Schottky Diodes

The level-shifting diodes in the A/D circuits required a consistent Schottky barrier height. As mentioned above, the use of a GaAs cap on the GaInAs/AlInAs MODFET heterostructure resulted in a Schottky barrier height higher than that of AlInAs with reduced leakage current. For this structure only minimum variations in Schottky barrier height were obtained from run to run.

Table 2.4 Specifications for the GaInAs/AlInAs MODFET

Material Properties	Target Range
Mobility	11-12X10^3 cm^2/V-sec
Sheet Carrier Concentration	2.0-2.2X10^{12} cm^{-2}

Device Parameters	Target Range
Drain Current (I_{dss}) at V_{gs} = OV; V_{ds} = 2.5V	400-450 mA/mm
Peak Transconductance (g_m) at V_{ds} = 2.5V	350-400 mS/mm
Pinch-off Voltage (V_p) at I_{dss} = 1 μA/μ	-2.0 V
Gate-drain breakdown voltage (Bv_{gd}) at -1.0 μA/μm	-10 to -15V
Drain-source breakdown voltage (Bv_{ds}) at Vg=0	3.5-5 V

Table 2.5. Specifications for the Passive Components

Mesa Resistor	350 ohms/square
Thin Film Resistor	5 ohms/square
Dielectric Films	SiO_2/Si_3N_4
Dielectric Breakdown	10^6V/cm

2.6 Thin Film Resistors

The final circuit design for the 3-bit A/D required both mesa and thin-film resistors. Table 2.5 lists the range of available resistance values. Mesa resistors were used for voltage dividers and current sources, while the thin film resistors acted as loads. Results from simulations showed that the tolerance on the thin film resistors needed to be better than $\pm$10%. By reducing the run-to-run variations in the sheet resistivity of the MODFET, we were able to meet this requirement. We evaluated both nichrome (>20 ohms/square) and titanium (5 ohms/square) thin-film resistors. Since titanium resistors gave better adhesion to the gold contacts at their ends, we chose Ti resistors over nichrome. We developed a technique for in-situ monitoring of the film resistance during deposition. We obtained 5 ohms/square with the required $\pm$10% tolerance by depositing and lifting-off the resistors.

2.7 Process Development

Although working circuits were not required until the second year of the contract, we modified our existing 2-bit A/D converter mask to facilitate the development of the process. The modifications included adding Schottky diodes, a high aspect ratio RTD, and a higher gain buffer amplifier. The mask contained several circuits, including 1-bit and 2-bit A/Ds that were designed to operate at effective sampling rates up to 1 GHz. The new process-development masks allowed us to run the entire sequence of processing steps, giving us invaluable information for designing the 3-bit, 10 GSps A/D planned for the second year of our program. After receiving the masks in December 1990, we processed several runs using optical gates and found all steps in the process worked as expected. The key results from these evaluations were:

- Our selective-epi process worked well. The MODFETs and 2-well RTDs on the dual heterostructure wafers had about the same electrical characteristics that we normally saw for these devices on single heterostructure wafers. Figure 2.20 shows four RTDs made on islands of selectively grown heterostructures.
- With the exception of the gate yield, the overall process worked well. We also ran through the complete process for the A/D converter using 0.5 μm gates written by e-beam at the University of Michigan (and two wafers at the NNF at Cornell University). We tested the FETs, RTD, buffer amplifier, and complete 1- and 2-bit A/Ds (see Figure 2.21) on-wafer. We measured the speed of the A/Ds, and found that they ran an order of magnitude slower than the simulations predicted. The main problem was that the load resistors in series with the RTDs were too large, causing a large hysteresis in the digitizer circuit.

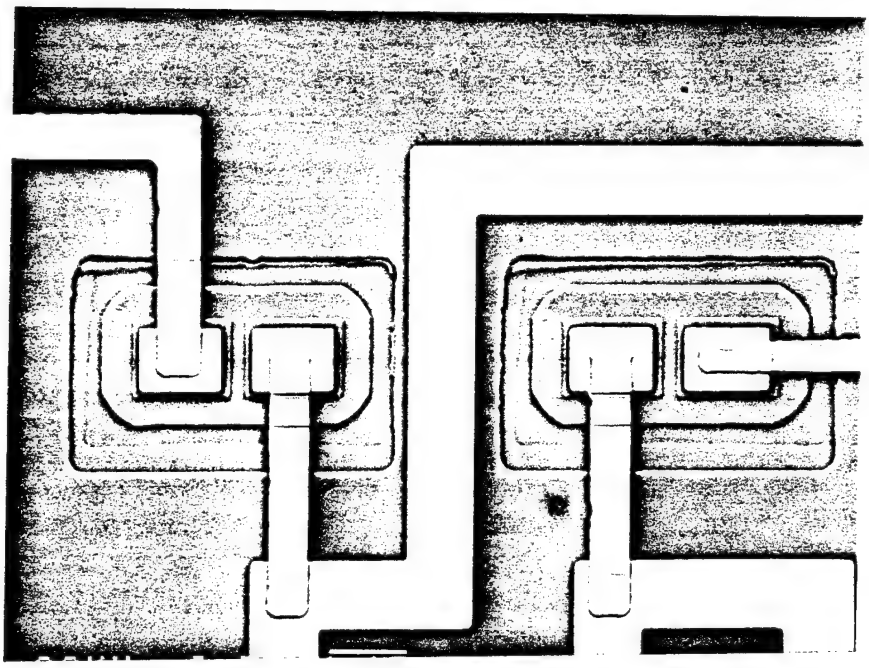


Fig. 2.20 This scanning-electron micrograph shows four RTDs made on islands of selectively grown heterostructure.

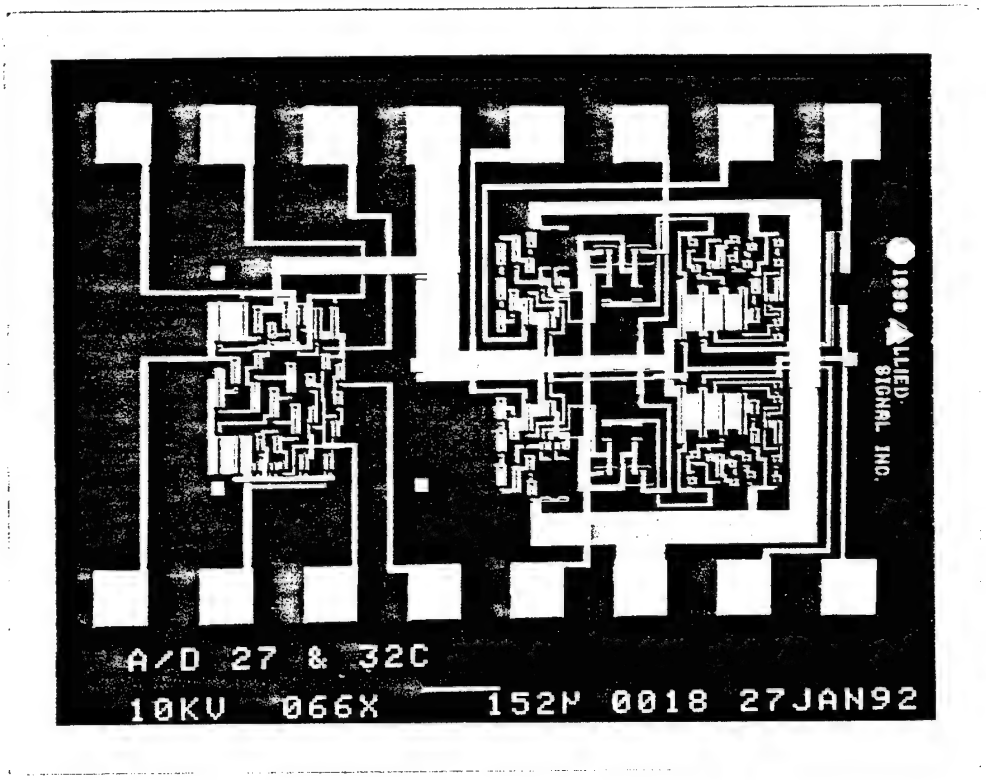


Fig. 2.21 This scanning electron micrograph shows the 2-bit A/D converter fabricated on dual-heterostructure substrate.

3.0 Design and Fabrication of the 3-Bit A/D

In this section various aspects of the design and simulation of three different RTD-based A/D converters are discussed. Also included are the fabrication sequence and high speed testing results for the 3-bit A/D converter.

3.1 3-Bit A/D Design and Simulation

3.1.1 Review of 3 different RTD-based A/D converters

The originally proposed RTD-based A/D converter for 4-bits is shown in Fig. 3.1. The input signal is divided into octaves by a chain of resistors. The low-output-impedance buffer amplifiers drive the RTDs. The 4-well RTDs serve two functions: 1) their peak-to-peak voltages are the reference voltages against which the input signal is compared, and 2) their negative-differential resistance eliminated the need for high-speed comparators. Each differential amplifier converts the response of a pair of 4-well RTDs into one-bit of a Gray-coded binary representation of the input signal. This architecture has the advantage of simultaneously digitizing all the bits at once, as in a conventional flash-type A/D converter. Another advantage is that the digitized output is automatically Gray-coded and does not require the complex circuitry flash A/D converters need to obtain the digital word output. Finally, the component count (and thus power consumption) is vastly reduced compared to that used in a flash A/D converter. A more complete description of the operation of this A/D converter is given in Ref. 2.

During the course of the contract, two new RTD-based A/D converter architectures were invented, the first of which is shown in Fig. 3.2, for 4-bits. This A/D converter

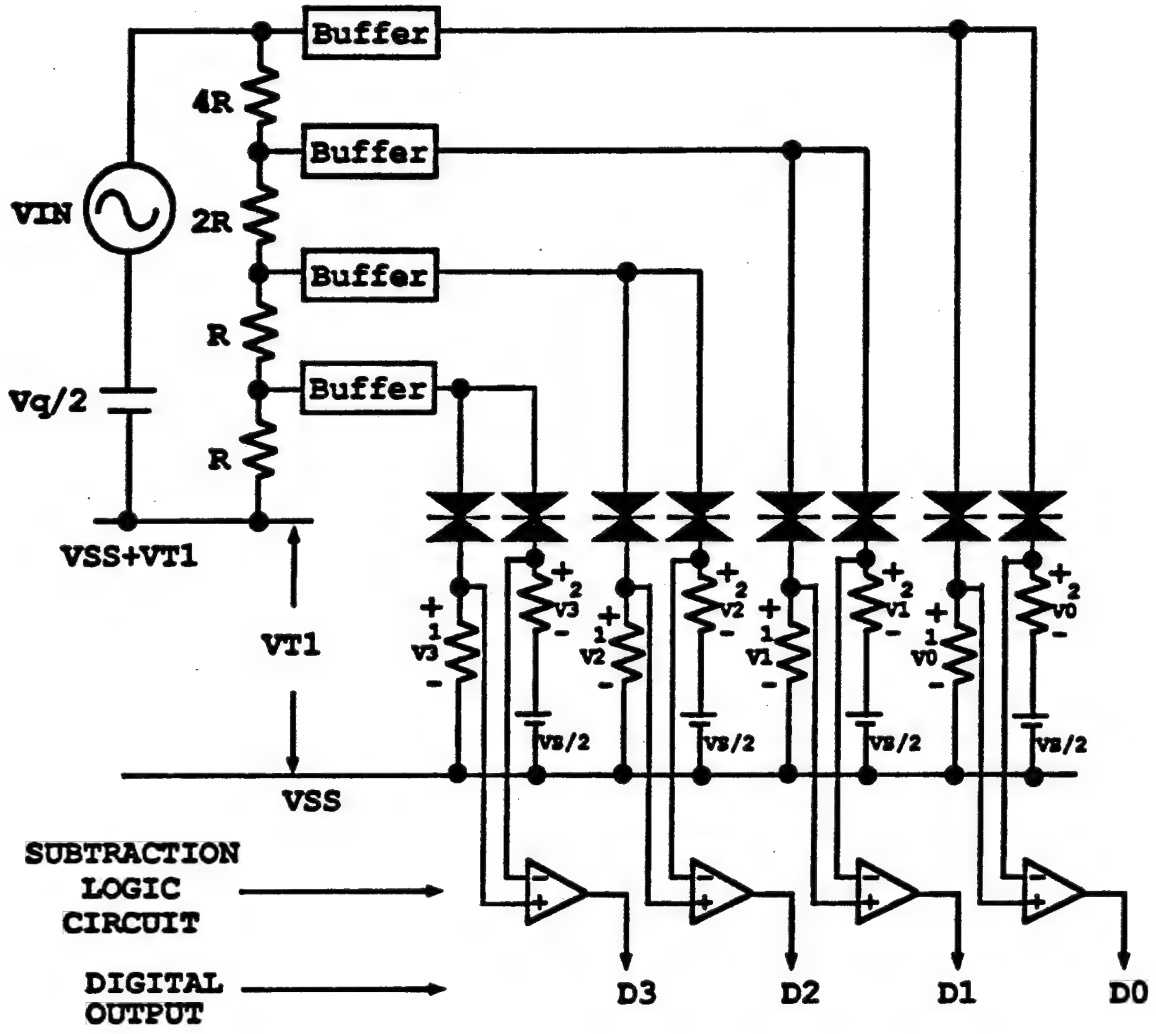


Fig. 3.1 The originally proposed RTD-based A/D converter shown for 4-bits. The multi-peaked RTD's "fold" the input signal and thereby quantize it [IEEE J. Solid-State Circuits 26, 145 (1991)].

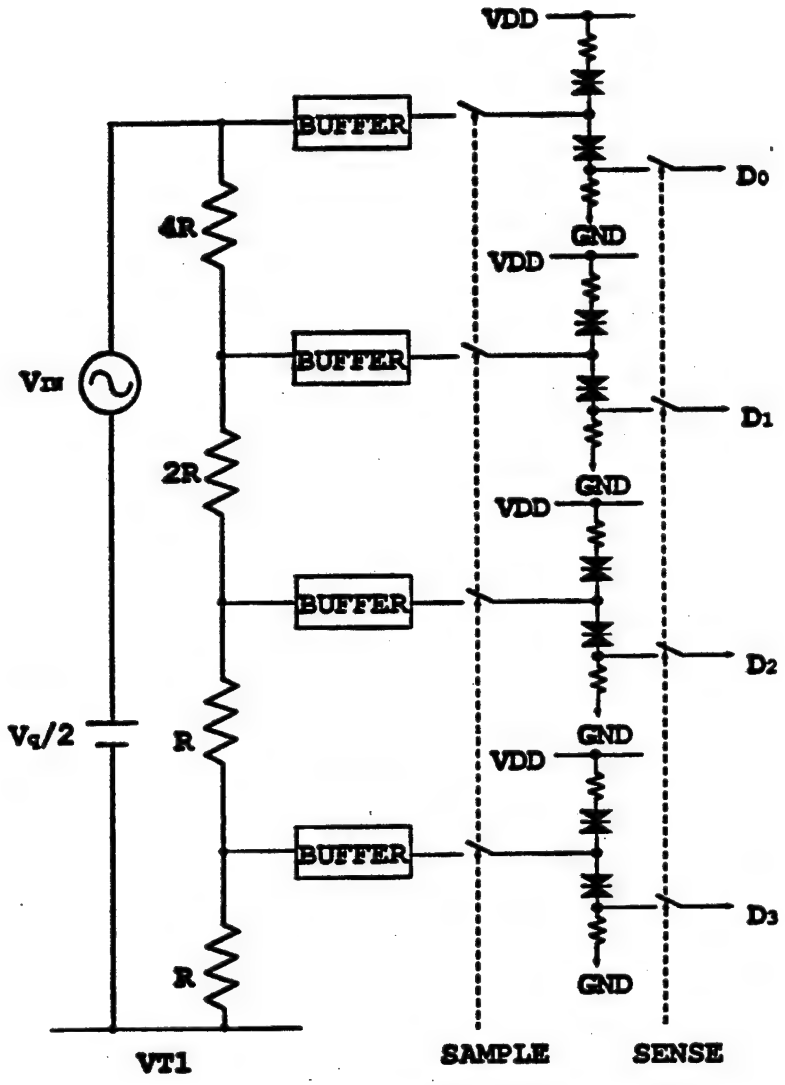


Fig 3.2. Second generation RTD-based A/D converter, shown for 4-bits, that uses an RTD pair to implement signal folding as well as a digital latching comparator that is shown in Fig. 3.3(a).

works quite differently from the one described above. The most unique aspect of this A/D converter is that it is self-latching by virtue of the pair of RTDs that act as driver and load and form a digitizer, as shown in Fig. 3.3 (a). The I-V characteristic of a 4-peaked RTD with another 4-peak RTD as a load is shown in Fig. 3.3 (b). Note that for m-peaked RTDs, there are m+1 stable states. These stable states form the basis for the self-latching action of this digitizer in this A/D converter. The operation of this novel A/D converter is more fully described in Ref.3.

The second RTD-based A/D converter invented during the course of this contract is shown schematically in Fig. 3.4, for 4-bits. Again, the principle of operation of this A/D converter is quite different from that of the preceding two A/D converters just described. In this design, the input signal is successively divided by two as in the previously described A/D converters. The signal then goes into a voltage-to-current folding subcircuit as shown in Fig. 3.5 (a). The signal folding is obtained from the RTD that is in series with the source of the MODFET. For a 3-bit A/D converter, a two-peak RTD is needed. The folded signal then goes to an RTD digitizer/latch. This digitizer/latch uses two one-peak RTDs in a driver/load arrangement. If I_0 is positive (negative) the digitizer will settle at P_0 (P_1) and latch there by virtue of the two stable points shown in Figure 3.5 (b). Note that in the previously described A/D converter, the digitizer was composed of two four-peaked RTDs to get both signal folding and latching, while in this A/D converter, the signal folding is done first, and then it is digitized/latched by a pair of one-peaked RTDs. The combined voltage-to-current folding circuit and comparator

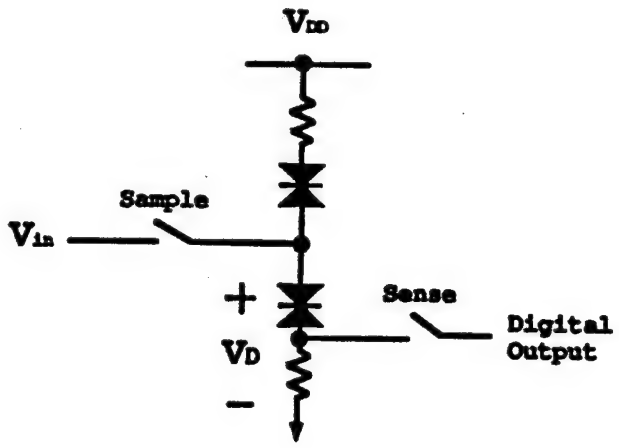


Fig. 3.3(a) RTD driver/load pair that serves as a digital comparator as well as a latch. The analog signal is also "folded" by the multi-peaked characteristic of the RTD that is shown in Fig. 3.3(b).

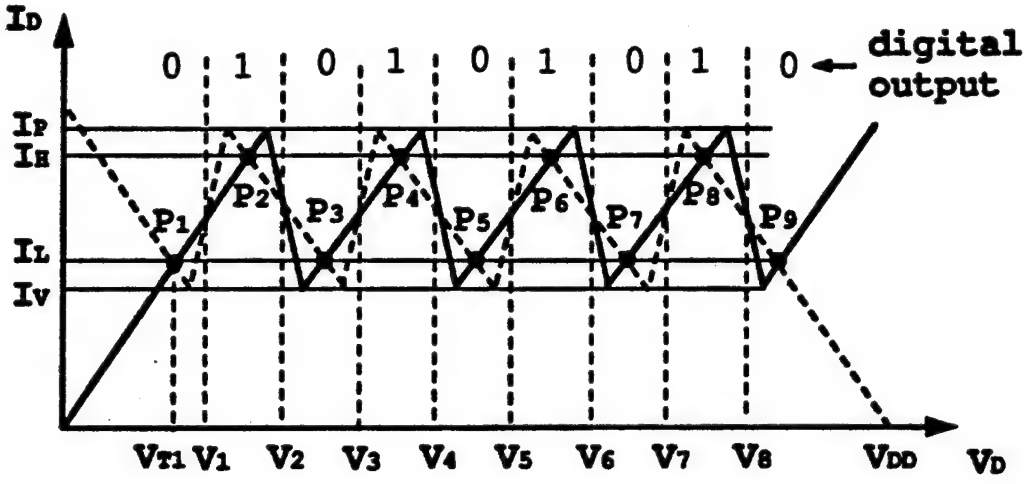


Fig. 3.3(b) Multi-peaked RTD characteristic that is used to fold the input signal. We achieved a hysteresis-free 4-peak I-V characteristic.

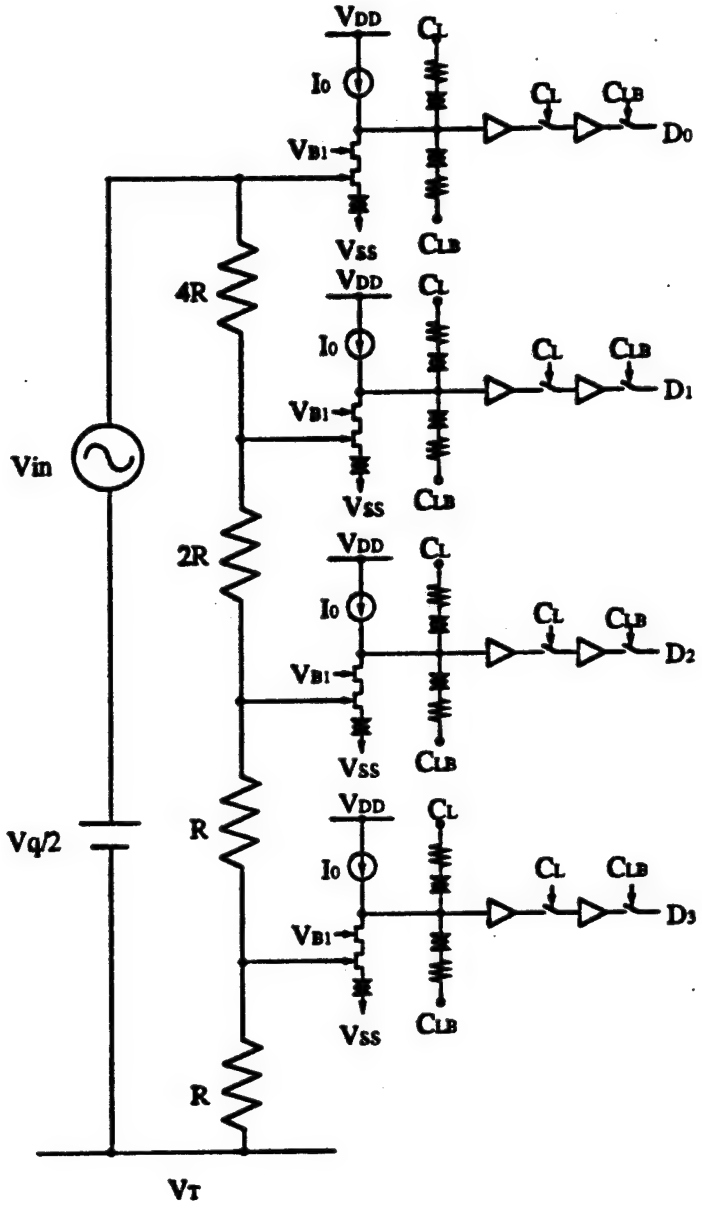
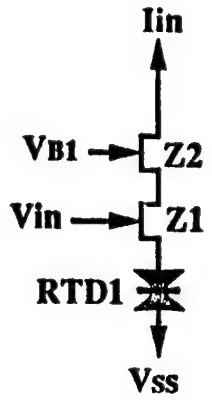
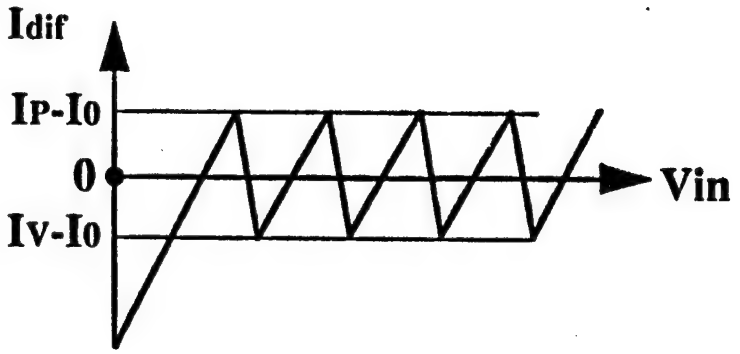


Fig. 3.4. Third generation RTD-based A/D converter, shown for 4-bits.



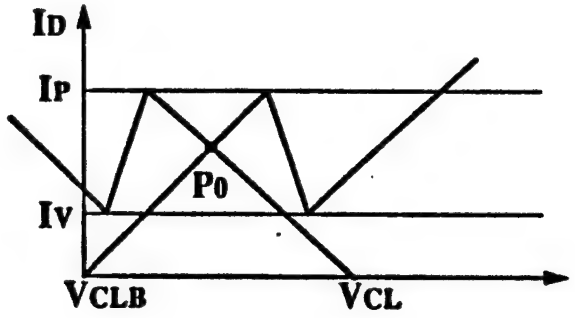


VOLTAGE TO FOLDING-

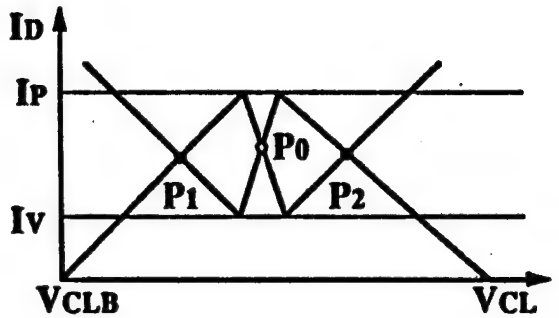
CONVERTER

TRANSFER CURVE OF I_{DIF}

Fig. 3.5 (a) Voltage-to-current folding subcircuit and transfer curve for I_{dss}.



I-V CURVES OF THE RTD PAIR IN THE RESET STATE



I-V CURVES OF THE RTD PAIR IN THE COMPARISION STATE

Fig. 3.5 (b). RTD-based comparator/latch

latch is called the current-mode digitizer and is shown in Figure 3.6. A more detailed description of the operation of this A/D converter is given in Ref. 4. The component count and power consumption for the 3-bit A/D converter is shown in Table 3.1.

Table 3.1 RTD-Based A/D Converter Component Count and Power Disspation.

Device/Circuit	3-BIT	5-BIT	6-BIT
RTD's	12	36	76
MODFET's	24	108	224
SCHOTTKY DIODES	15	90	185
RESISTORS	15	39	76
TOTAL	66	273	561
POWER (W)	0.34	1.1	2.4

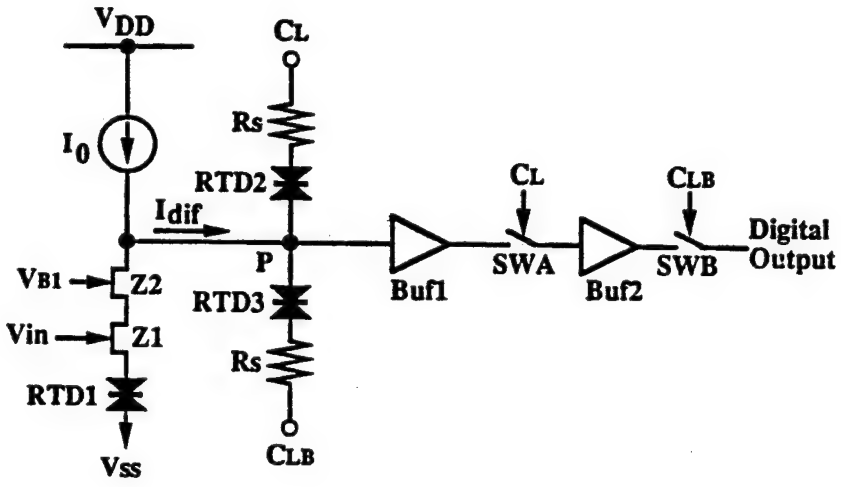


Fig. 3.6 Current-mode digitizer circuit.

3.1.2 Logic Type (depletion-mode MODFETs)

In order to keep the processing tractable, depletion-mode MODFETs were used for the level-shifter/buffer amplifiers (BFL) and the voltage-to-current folding circuits. Circuits that use depletion-mode MODFETs have less stringent requirements on the device uniformity than an enhancement/depletion approach but require two power supplies and level shifting, and consume more power. A more complete description of the MODFET and its characteristics are given in Section 2.4.

3.1.3 RTD Modeling

The RTDs were simulated using a model (shown in Fig. 3.7) we developed for the multi-well RTD (Ref. 5). It is based on decomposition of the RTD's I-V characteristic into a piecewise linear curve. The model uses a voltage-controlled switch that is supported in SPICE3 or PSPICE. The model includes capacitance that was extracted from small-signal, on-chip measurements of the RTD's S-parameters at microwave frequencies at various dc bias points. The model was used to verify the low-frequency functional operation of the A/D converter and was also used to show that the RTDs can switch on the order of several ps and do not limit the ultimate speed of the A/D converter. A complete description of the RTD structure and characteristics is given in Section 2.3.

3.1.4 MODFET Modeling

A large-signal model of the AlInAs/GaInAs-based MODFET was developed for simulating the operation of the various subcircuits (level shifters/buffers, voltage-to-current folding, etc.). SPICE3 and PSPICE contain a GaAs MESFET model which was found to be suitable for modeling the In-based MODFET. Because the MODFET has a bell-shaped transconductance as a function of gate voltage as opposed to the MESFET

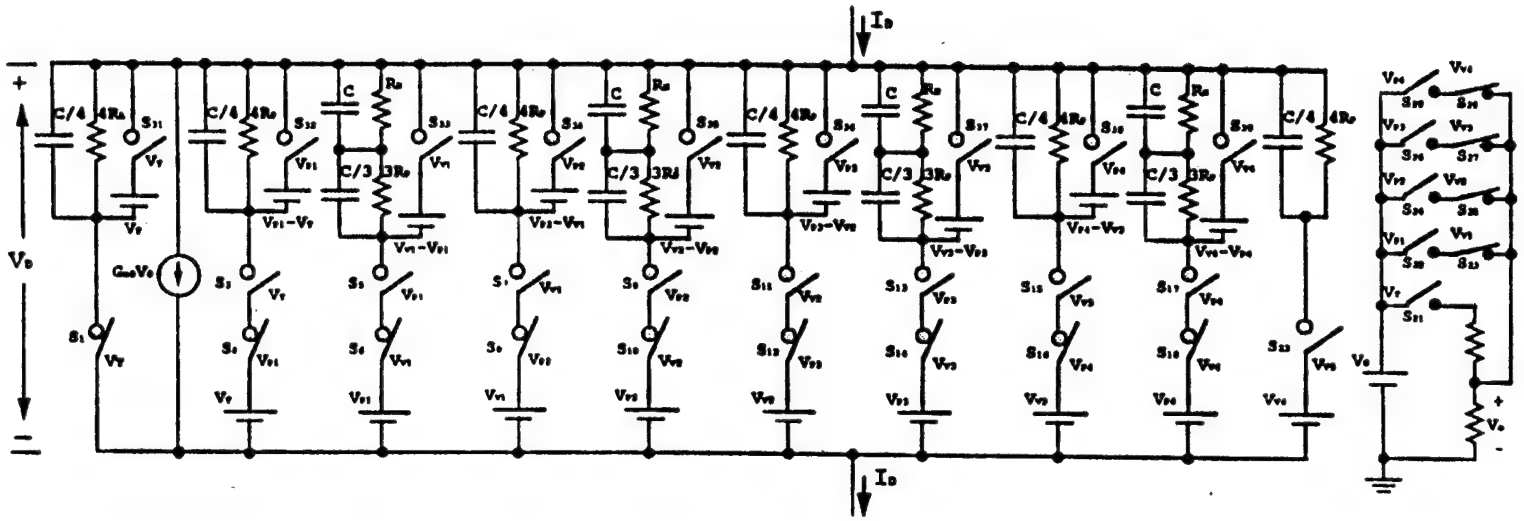


Fig. 3.7 Large-signal RTD model used to model the multi-peaked RTDs in SPICE3 circuit simulations. The model uses the "switch" function that is part of SPICE3 and PSPICE.

which has a linear transconductance with gate voltage, a model consisting of two parallel MESFETs was used and found adequate to model the MODFET (see Ref. 6).

During the circuit simulation of the A/D converters, the I-V characteristic of a nominal 0.5 μm gate length MODFET was used. While the switching speed of the device was found adequate for the 8-bit sampling at 4 GHz, it's f_t was too low for the performance needed for the 3-bit sampling at 8 GHz. We therefore decided to develop a 0.25 μm MODFET which was expected to have a much higher f_t and be able to switch at rates that were needed for the 4-bit A/D converter. While the 0.25 μm e-beam written gate device did achieve an f_t of 85 GHz, we found that it's breakdown voltage was less than 3.0V, which was too low for use in the A/D converter. As a compromise, we decided to use the 0.5 μm devices for both the 3- and 6-bit A/D converters that had lower sampling rates than the originally proposed 4- and 8-bit A/D converters.

3.1.5 Testability and Test Structures

Testing the A/D converter and debugging non-functional or poorly performing circuits was a difficult task at the high frequencies involved. The mask set was designed to make these jobs as simple as possible. The mask set included a process control monitor that had: 1) individual MODFETs, RTDs, and Schottky diodes; 2) test structures to measure parameters such as ohmic contact resistance, 1^{st} and 2^{nd} metal interconnect resistivities, gate resistivity, thin-film-resistor ohms/square, contact resistances between various layers, cross-overs between 1^{st} and 2^{nd} interconnect metals, etc.; 3) individual subcircuits that could be on-wafer tested at high frequencies; and 4) separate resistor ladders like those used in the input voltage divider. All the test structures were designed for on-wafer probing, even at the highest frequencies. We

found that these test structures were invaluable in trouble shooting the devices and circuits. Figure 3.8 shows a plot of the process control monitor that contains these test structures.

3.2 3-bit A/D converter Fabrication

We ordered and received all eleven masks for the new 3-bit and 4-bit A/Ds. We reproduced the RTD characteristics that were used for the design of the A/D. We grew about 30 dual-heterostructure wafers. The processing sequence of the 3 and 4-bit A/D converter is shown in Figure 3.9. Figure 3.10 (a) and (b) shows a scanning electron micrograph of the 3-bit and 4-bit A/D converter fabricated on a dual-heterostructure wafer. We averaged about one complete run of A/D's per week. Initially, various processing problems caused low yields. These problems included: open gates, poor step coverage, poor metal contacts and random defects causing opens in the metal lines. We systematically identified and solved these problems and made several modifications to the process. We used both pyrolitic CVD and ECR-plasma deposited SiO_2 as intermetallic dielectrics, and wet chemical etching of vias. In order to get acceptable yields with 0.5 μm gates, we used direct-write e-beam lithography for the gate level. We worked with the University of Michigan, Cornell University (2-wafers) and the Microelectronics Research Laboratory (NSA) for e-beam lithography. While the quality of the work was good, timely service was a problem with all three facilities and points out the need in this country for a good commercial service for e-beam lithography.

We worked with the mask supplier to improve our process for cleaning the gate mask, which resulted in higher yields for optical (contact printing) 0.5 μm gates. We

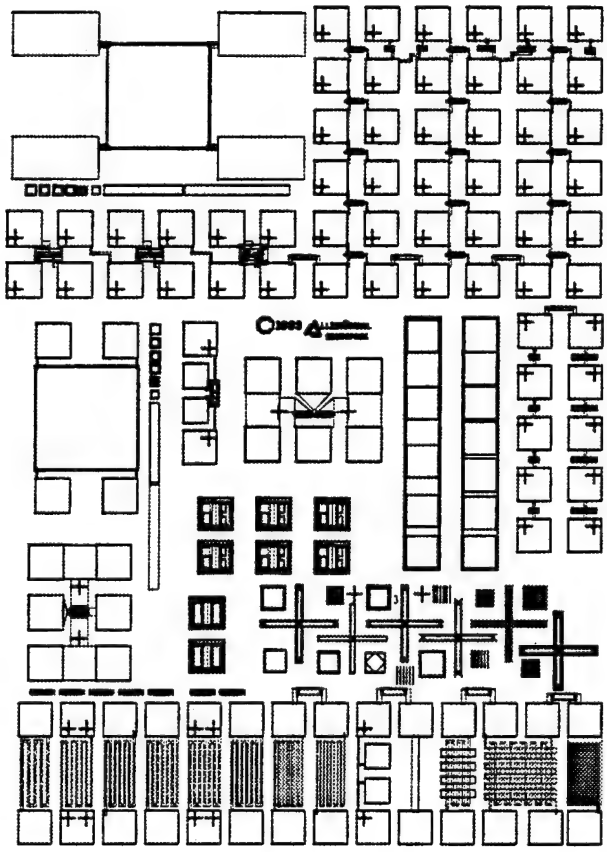


Fig. 3.8 Plot of the PCM (process control monitor) that was used to characterize the process for the fabrication of the A/D converters.

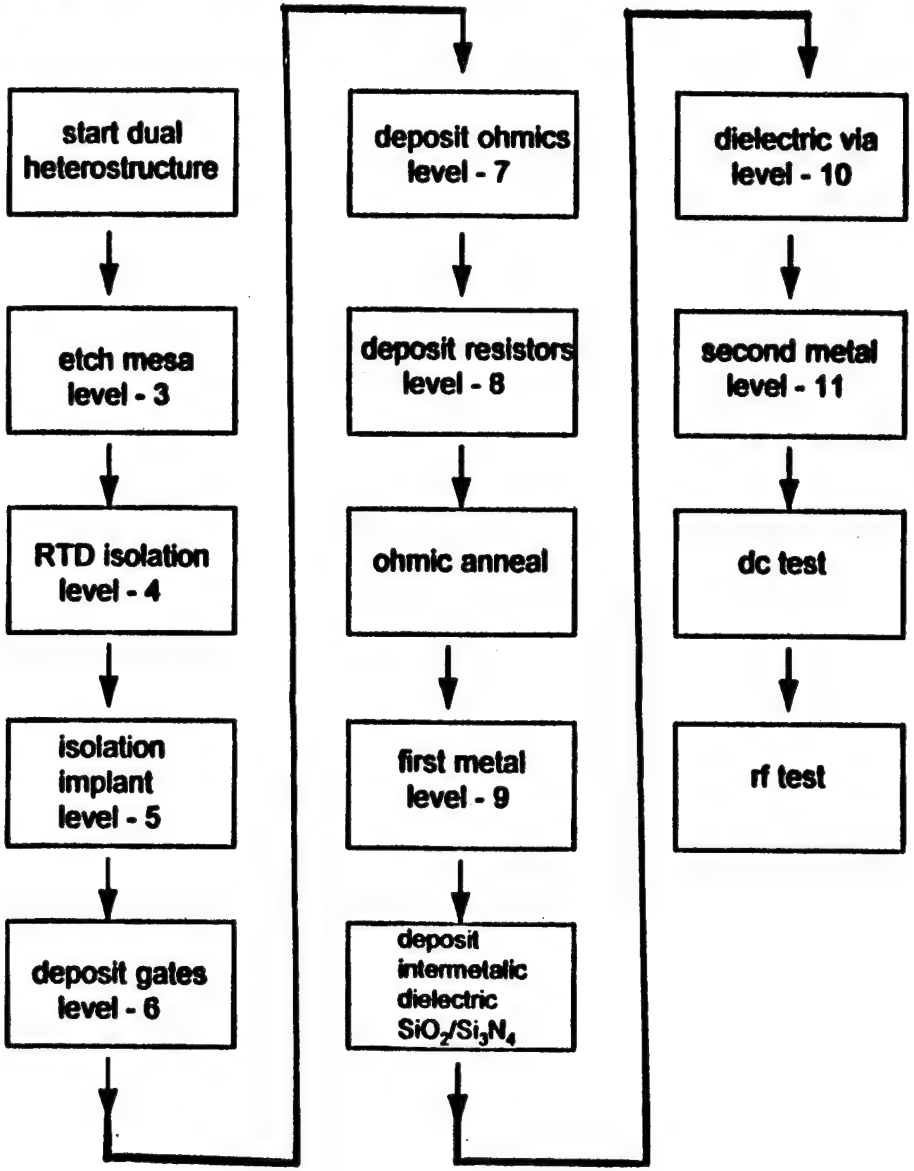


Fig. 3.9 This processing sequence was used for fabricating the monolithic A/D converter.

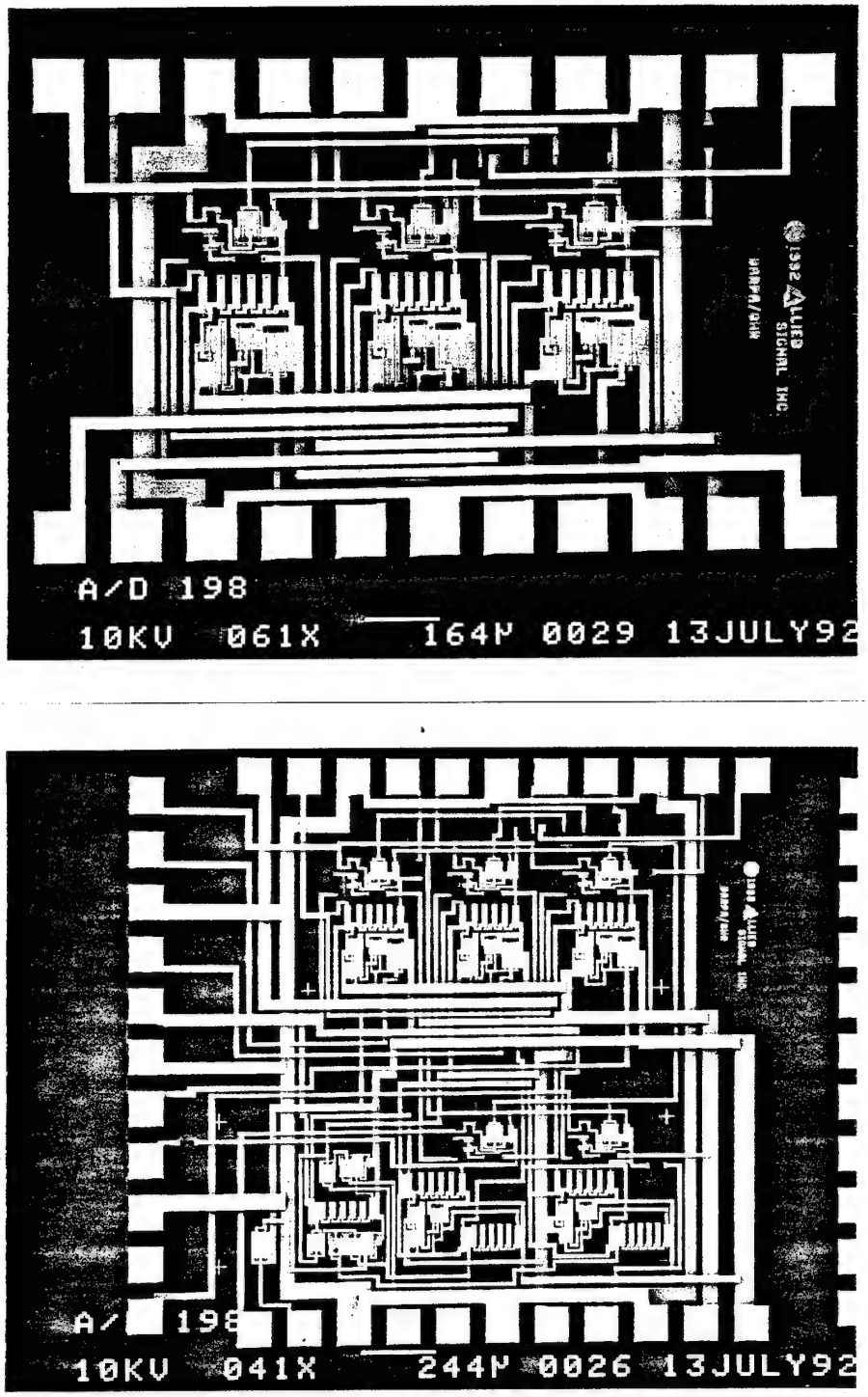


Fig. 3.10 Scanning-electron micrograph from one of our processing runs of the A/D converter showing (1) 3-bit A/D and (2) 4-bit A/D converter.

solved the few device problems that surfaced during the earlier runs: low I_{dss} for the MODFETs and higher current for the RTDs after the growth of the MODFET. To overcome these problems, we routinely grew a calibration sample and processed RTDs and adjusted the thickness of the barrier/well to meet the required current. We traced the low I_{dss} of the MODFET to processing problems and we modified the process slightly. The final process for making the A/Ds gave acceptable yields for running in a research cleanroom Yields undoubtedly could be greatly increased by further tuning of the process and instituting the disciplines used in a production cleanroom. A total of 35 process runs of 3-bit and 4-bit were completed.

3.3 Testing High-Speed A/D's

3.3.1 On-wafer probing/low speed testing/high speed testing

The 3- and 4-bit A/D converters were layed out so that they could be tested on-wafer at high-frequency using standard Cascade probes.The use of on-wafer probing resulted in savings in terms of time and money compared to dicing and packaging each circuit individually for testing. The 3-bit A/D converter required two 11-pin high-speed Cascade probes while the 4-bit required three 11-pin high-speed probes. Because of the high-speed nature of the circuits being tested, and the large number of signal and power connections needed, this on-wafer test setup was one of the most complex ever assembled and represented state-of-the-art in circuit testing. Pictures of the test setup are shown in Figures 3.11(a) and 3.11(b).

Three approaches were used in testing the A/D converters. First, a visual inspection was made of the individual circuits on the wafer so that circuits with obvious defects

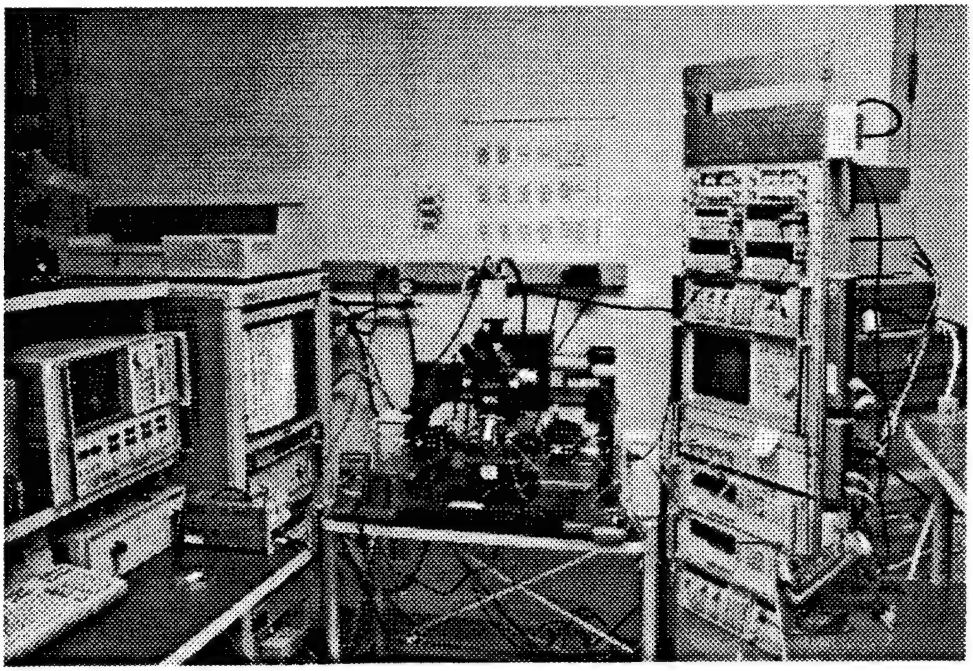


Fig. 3.11(a). On-wafer, high-speed test setup for testing the A/D converters

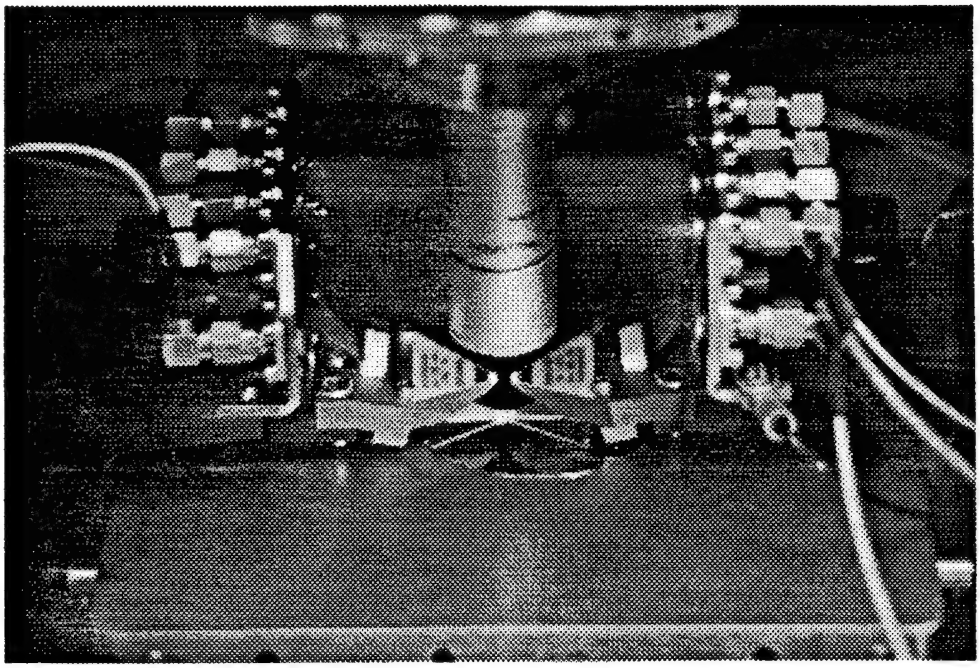


Fig. 3.11(b). High-speed probes in contact with a 5-bit A/D converter during testing.

could be screened out and not tested further. Such defects included FETs with open gates, FETs with shorted gates, missing metal interconnect, shorted interconnects (where lift-off was incomplete), and so on. Another test that was done prior to ac testing was completing a dc test of the PCM. This would allow us to characterize the active devices (FETs, RTDs, and Schottky diodes) and to find defects in the process that were not visible, such as shorts between metal 1 and metal 2, bad contacts between layers such as metal 1 to metal 2, gate metal to metal 1, etc. Assuming the devices and test structures passed these preliminary tests, the circuits were then tested under full bias in the high-speed test setup.

Second, to verify the functionality of the A/D converter, initial circuit testing was done at low input frequency and sampling (clock) rate. Because of the large number of power supplies, finding the proper biasing points simultaneously was one of the biggest challenges to getting the A/D converters to function. For example, the 3-bit had 7 dc power supplies and 3 current sources, while the 5-bit had 14 dc power supplies and 9 current sources.

Finally, functional circuits which passed the pre-screening would be tested at the highest sampling rate of about 2 GHz, first at low input sample frequency, and then at high input sample frequency. During the high-speed testing, the dc biases would again have to be adjusted to get the desired functionality. This bias adjustment process was quite time consuming and very problematic.

Researchers at the University of Maryland (Professor Lin and Hao Tang) developed a high-speed tester for testing of the RTD-based A/D converter that is shown in Fig. 3.12. A signal generator provides a high purity sine wave output at up to the sampling.

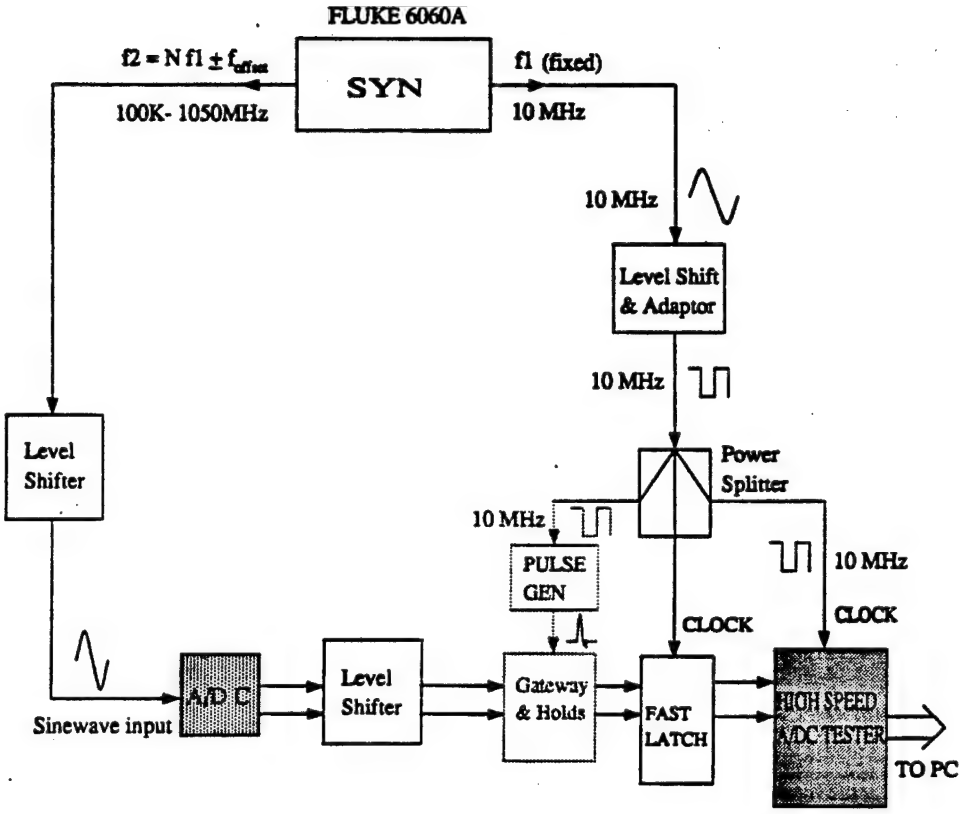


Fig. 3.12. Block diagram of high-speed A/D test setup.

frequency f_1 for the A/D converter. A free-running sine wave with frequency f_3 is used as the input to the A/D converter; this frequency is limited by the Nyquist sampling theorem. Typically, f_3 is on the order of a few hundred MHz. A Colby clock driver is used in shaping the original sine wave into a square wave with fast rise and fall times In addition, it provides the sampling clock signals to the A/D converter. High bandwidth fanout buffers are used to distribute the clock signals to the D-flipflops while preserving the signal's rise and fall time characteristics and logic levels. The frequency divider is an N stage (N=7 in our case) high-speed counter which will divide the original frequency by a factor of 2^N to give a signal at f_2. The divided signal is then fed into another fanout buffer and is used to synchronize an existing low-speed tester with the high-speed tester. A more complete description of this test setup is given in the Masters thesis of Hao Tang, listed in the Publication Section of this report.

3.3.2 Testing the 3-bit A/D Converter

As mentioned in the previous Section, one of the biggest challenges to get the A/D converters to work was to find the proper biasing points simultaneously such that all outputs had the proper timing and wave shape. We attribute this tedious adjustment procedure to variations in the device characteristics that were due to both process variations and to variations in the electronic properties of the heterostructures. Figure 3.13 shows the best result we achieved for the 3-bit A/D converter at a 2 GHz sampling (clock) rate.

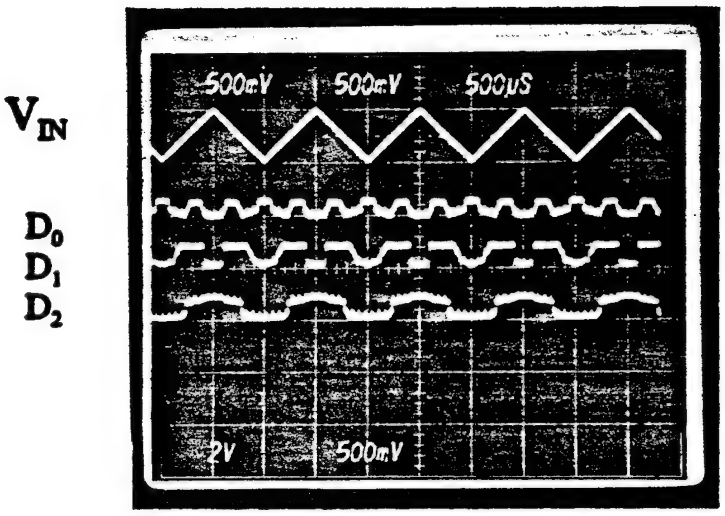


Fig. 3.13 Output from the 3-bit A/D converter at a 2 GHz sampling rate.

4.0 Design and Fabrication of 5 and 6-Bit A/Ds

4.1.1 Hysteresis Limiting the Number of Peaks in the RTD

Ideally, we would have liked to extend the idea of signal folding to achieve A/D conversion at a resolution of 6 bits, in a way that was similar to that which was done for the 3-bit A/D converter. However, to get 6-bits of resolution, a 16 peak RTD would have been needed and to get 5-bits of resolution, an 8 peak RTD would have been needed (see Table 4.1). We have empirically found that the most peaks we can get are 4, and beyond that, the I-V characteristic exhibits hysteresis. Hysteresis in the I-V characteristic would result in large quatization errors in the A/D conversion process, and hence its presence is not acceptable. Using a 4-peaked RTD would allow a 4-bit A/D converter to be built and this could serve as the basic building block for A/D converters with resolutions greater than 4-bits. While a hysteresis-free 4-peak device was made, the device did not have enough negative differential resistance to be used in a 4-bit A/D converter. The voltage span required to achieve hysteresis free 4-peak RTDs was greater than BV_{ds} of the MODFET. We believe however, that by using Sb-based RTD's, a 4-peaked device could be made that would be suitable for 4-bit A/D conversion.

Table 4.1 RTD-Based A/D Converter - Relationship Between Resolution and RTD Peak #

m = # of peaks in RTD characteristic

n_S = # of useful stable points in RTD driver-load pair

n = # of bits of resolution

$n_{states} = 2^n$

m' = # comparators in a flash A/D converter = $2^n - 1$

m	n_S	n	n_{states}	m'
1	2	2	4	3
2	4	3	8	7
3	6		12	
4	8	4	16	15
5	10		20	
6	12		24	
7	14		28	
8	16	5	32	31

Relationship between m and n is: $m = 2^{(n-2)} = 2^n / 4$.

(Note: For an n-bit RTD-based A/D converter, the # of RTD's needed is n or one m-peaked RTD per bit.)

4.1.2 Approach to Achieve 5 or 6-bits by Using 3-bit A/Ds

Because of the hysteresis problem described in the previous section, the basic building block for A/D conversion was 3 bits, which required a two-peak RTD. The block diagram of the 5-bit A/D converter is shown in Fig. 4.1. The three most

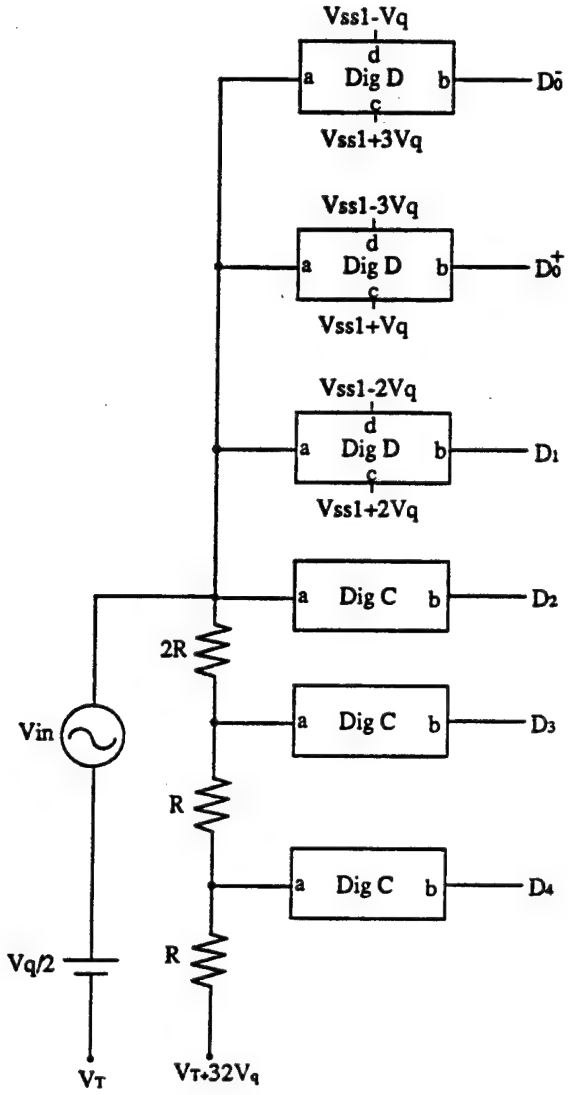


Fig. 4.1. Block diagram of the 5-bit A/D converter.

significant bits (D_4, D_3, D_2) were obtained by using the basic "3-bit" A/D converter block already described. The least two significant bits were obtained from D_2 by shifting the threshold of the quantizers to get a quantizer for the least two significant bits (D_1 and D_0) using circuit blocks that contained two current mode digitizers and an XOR gate that combined the digitizers outputs. These circuit blocks are designated as Diagram "C" or "D" in Fig. 4.2. It is worth emphasizing that for each bit above three, the complexity of the A/D converter doubles, so a 5-bit A/D converter has about four times as many components as the 3-bit and consumes about four times the power. This information is summarized in Table 3.1.

The realization of the 6-bit A/D converter uses a technique that is similar to the method just described for the 5-bit A/D converter. To achieve 6 bits of resolution, two 5-bit A/D converters were combined as shown in Fig. 4.3. The least significant bit, D_0, would be generated by obtaining the exclusive-or (XOR) of D_{0+} and D_{0-}. This XOR function was put off-chip to reduce the complexity of the circuit and could be conveniently be obtained using either a digital scope or a conventional analog oscilloscope. The component count and power consumption of the 6-bit A/D converter is shown in Table 3.1.

4.2 Processing and Testing 5 or 6-Bit A/D Converters

4.2.1 Processing the 6-bit A/D Converter

We ordered a new mask set for fabricating 5-bit and 6-bit A/Ds. The mask (shown in Figure 4.4) included circuits for 1-bit, 3-bit, 5-bit and 6-bit A/Ds along with process control monitors for checking various steps in the process. Based on what we learned from the 3-bit A/D's we made minor modifications and improvements in the processing

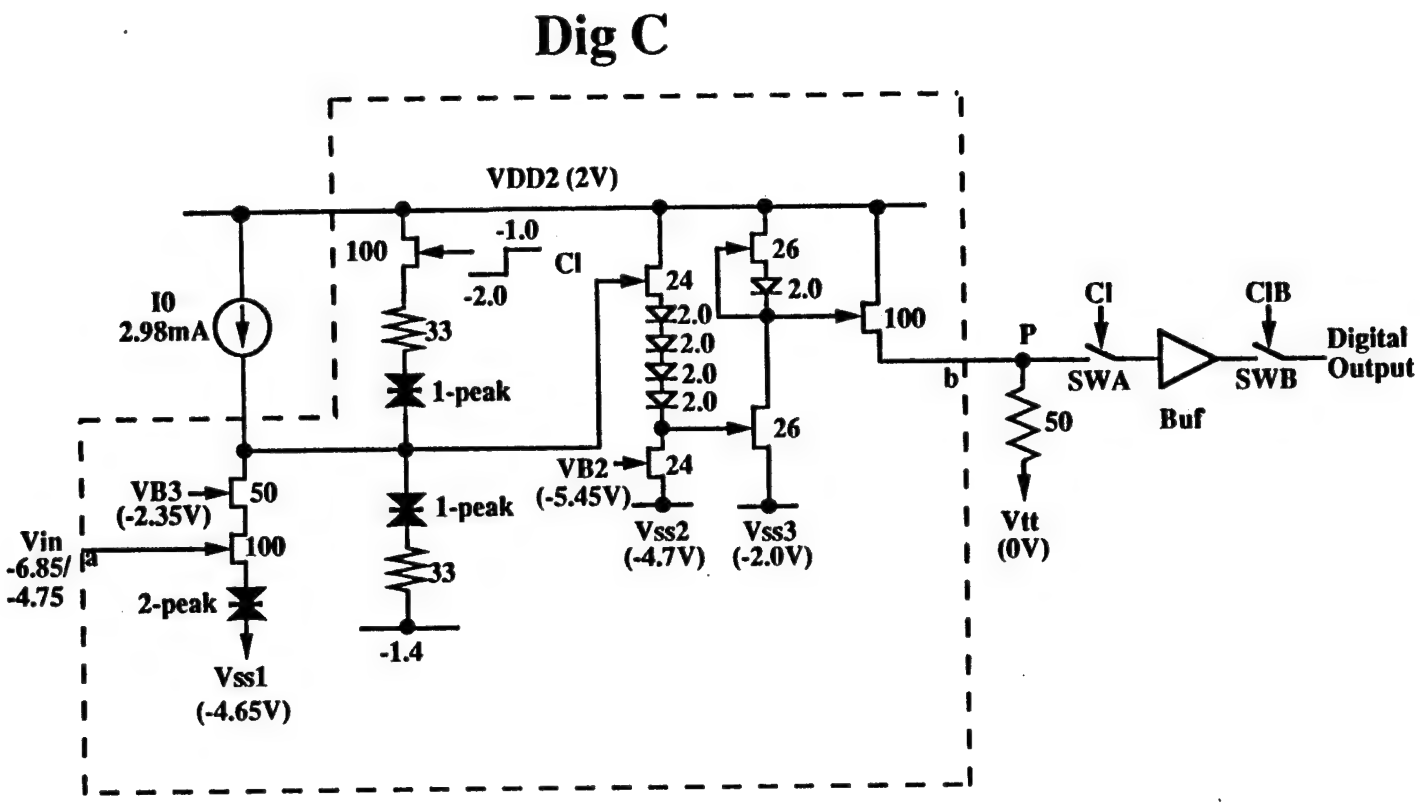


Fig. 4.2(a) Subcircuits C of the 5-bit A/D converter shown in Fig. 4.1

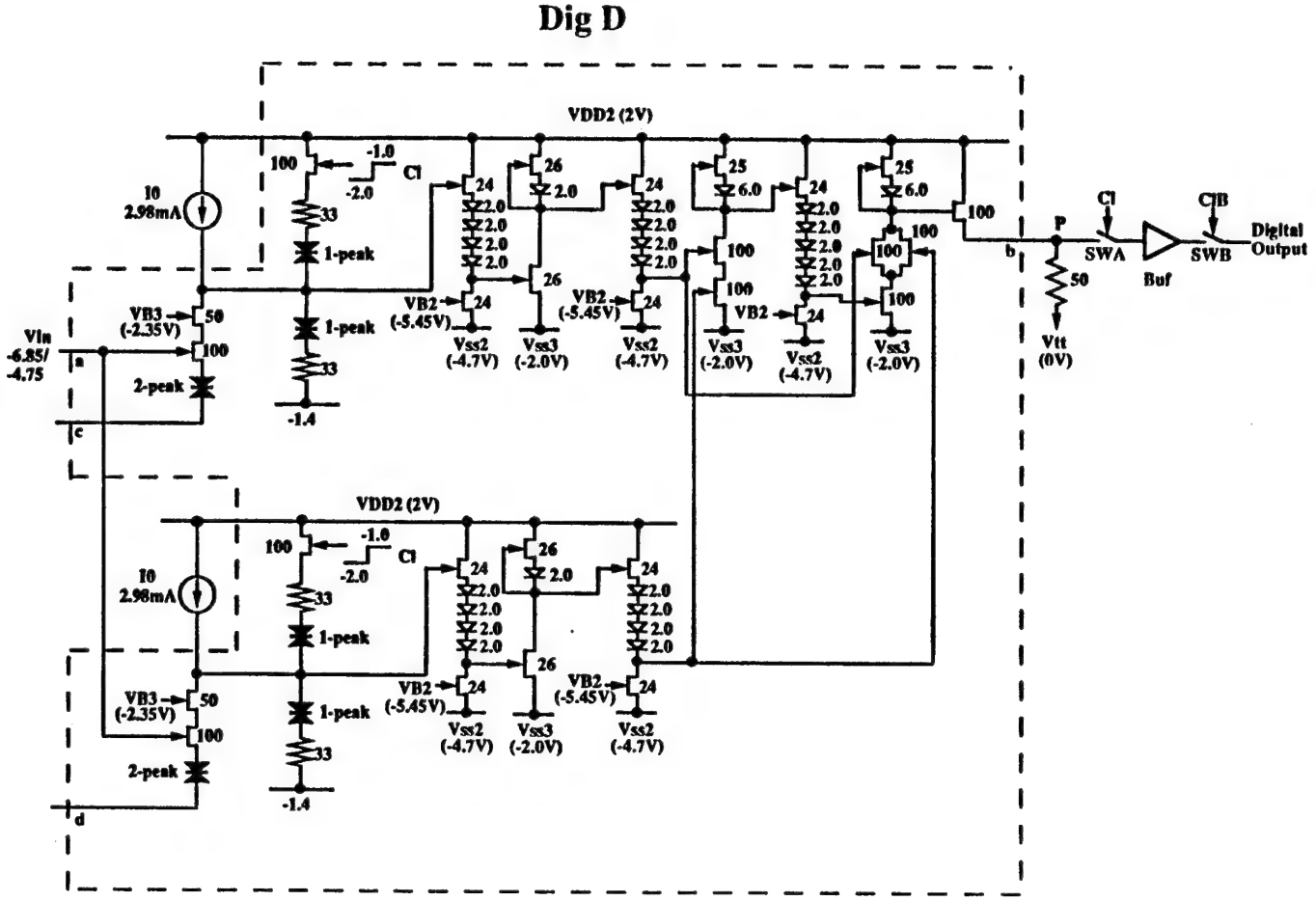


Fig. 4.2(b) Subcircuits D of the 5-bit A/D converter shown in Fig. 4.1.

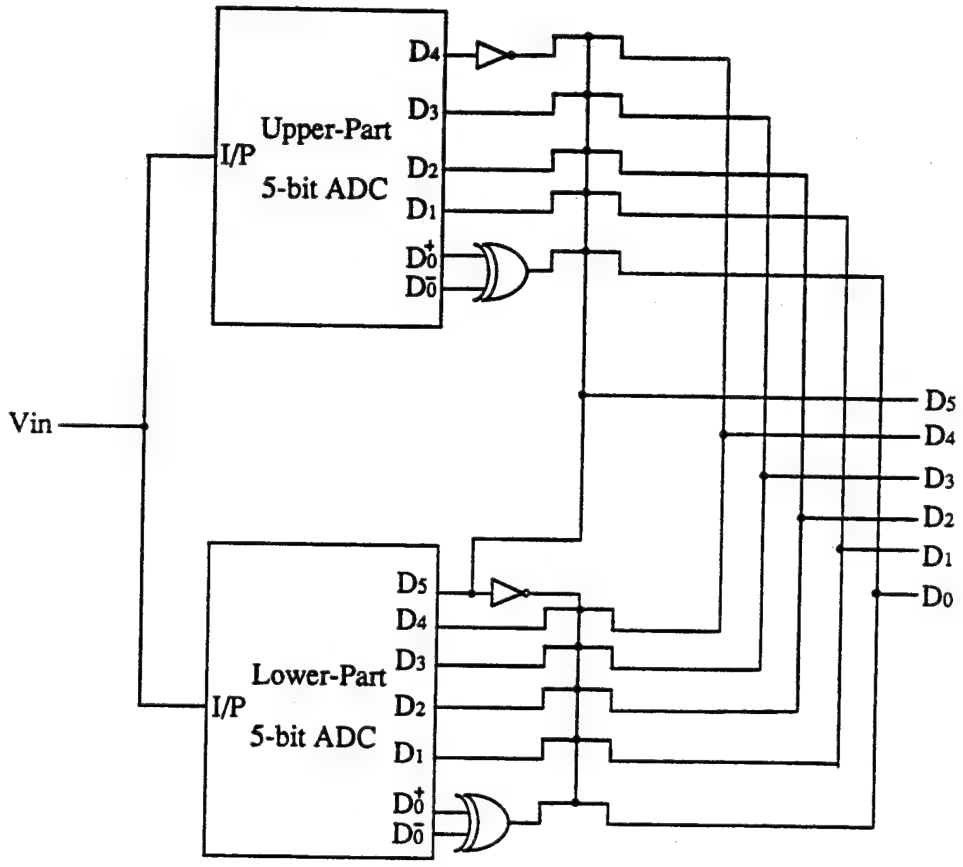


Fig. 4.3. 6-bit A/D converter using two 5-bit A/D converters.

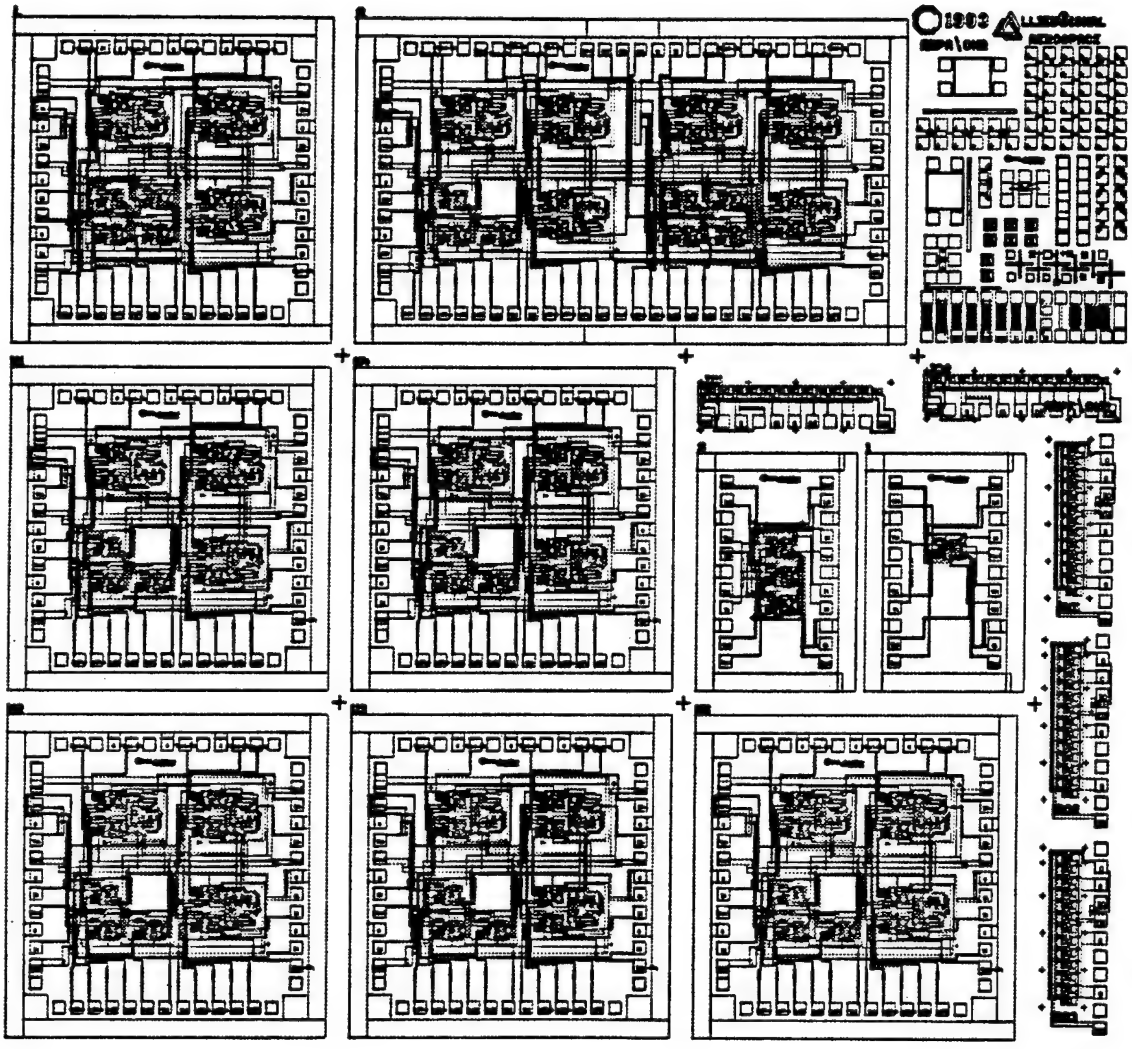


Fig. 4.4 Layout of the 5-6 bit A/D converter

of the 5- and 6-bit A/Ds. We also changed the inter-metallic dielectric from SiO_2 to Si_3N_4. The sequence for processing A/Ds is shown in Figure 3.9.

After processing a few wafers, testing of the circuit showed a significant reliability issue with the Si_3N_4 intermetallic dielectric film deposited by ECR-plasma CVD system. When the bias voltages were applied to the circuit, bubbling of the Si_3N_4 started after a few minutes and finally breakdown occurred at crossovers. We improved the reliability of the films by adjusting the deposition parameters. With a modified metalization scheme and optimized deposition parameters, breakdown voltages as high as 30 V for greater than 60 minutes were measured on these films (300 nm thickness) which exceeded the requirements for the A/D circuit.

We made several complete runs (about 50) of 5- and 6-bit A/Ds and used both optical and e-beam written gates. The e-beam gates were written at MRL. In spite of a few minor problems in the mask and processing (mentioned above) we had fully functional monolithic 5-bit A/D circuits. Figure 4.5 shows an island of RTDs and Figure 4.6 shows a 5-bit A/D converter fabricated on a dual-heterostructure wafer.

4.2.2 Testing of 5-bit

The testing of the 5-bit A/D converter was a scaled up effort of that used to test the 3-bit A/D converter. For the 5-bit A/D converter, three 11-pin high-speed probes were used along with one 12-pin dc needle probe. The best result for the 5-bit A/D converter is shown in Fig. 4.7, where all five bits are functioning. The clock rate for this result was about 300 MHz and the input signal frequency was about 50 MHz. The limitation on the clock rate is due to the limitation of the on-chip XOR circuitry due to signal jitter.

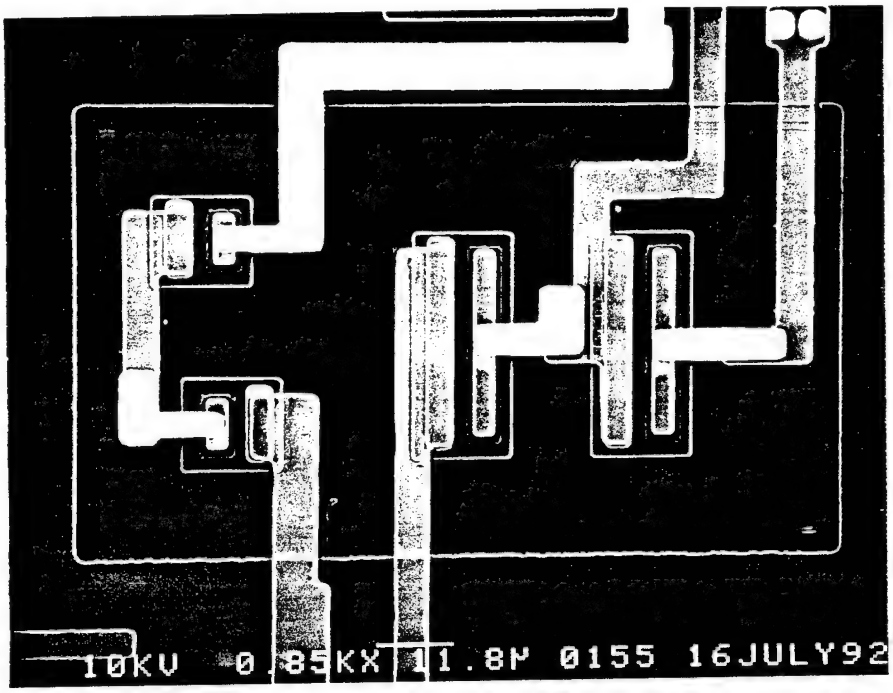


Fig. 4.5 This SEM photo shows four RTDs made on selectively grown heterostructures for A/D converters.

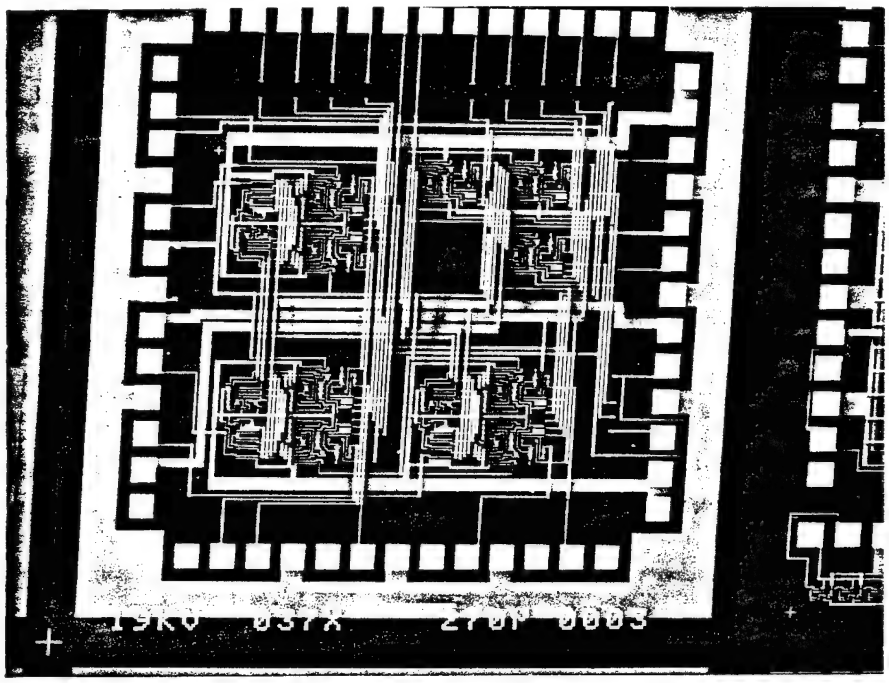


Fig. 4.6 This SEM Photo shows a 5-bit A/D converter.

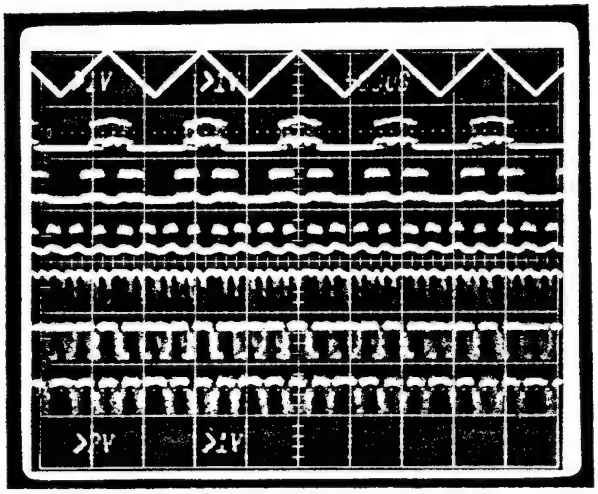


Fig. 4.7 Output from the 5-bit converter showing that all bits are functioning.

We think that by putting a latch between the RTD comparator and the XOR gate, this jitter problem would not exist and clock rates that were used to test the 3-bit A/D converter could then be used with the 5-bit.

The testing of the 6-bit A/D converter would necessitate its mounting into a fixture as the large number of pinouts (60) would make high-speed on-wafer probing impractical. Because this type of testing is very costly, and would require a separate development effort, no attempt was made to put the 6-bit A/D converter into a fixture for testing, as this level of testing was beyond the scope of the project.

5.0 Technology Insertion

5.1 Meetings with DoD on A/D requirements

Several visits were made to various DOD laboratories in order to determine their A/D converter needs. In particular, visits were made to the Naval Research Laboratory(NRL) and to the Air Force Rome Labs-Griffiss. At NRL, the primary contact was Jim Constantine (Airborne EW) and a second contact was Dan Goodman (Digital Receivers). At Air Force Rome Labs - Griffiss, the primary contacts were with Peter Leong (Radio-Signal Processing), Dwayne Allian (Digital Receivers), and Capt. Rich Linderman (Radar-Signal Processing). In addition, we had several conversations with Jonh David and John McCorke of Harry Diamond Labs regarding their A/D converter needs. Also, we had brief discussions with Lutz Micheel of Wright Labs regarding our A/D converter program and how it compared to the Rockwell A/D program, which Lutz had been monitoring for the last six years. We also talked to David Sharpin (Passive ECM Branch of the EW Division) at Wright Labs regarding applications of high-speed (> 1 GS/s), low resolution (< 10 bits) A/D converters.

For the majority of the users we have talked to, speed was an issue but accuracy was an equally important issue. An accuracy of 10 bits seems to be their minimum useable performance; 12-14 bits of accuracy was greatly desired regardless of the speed. The applications seem to divide into two groups: 1) those that require real-time processing of digital data from the A/D and 2) those that can tolerate the delay of off-line processing. The number of applications from the first group seem to outnumber those in the second. Those applications in the first group were limited not only by the speed of the A/D but also by the speed of the digital computer; for such applications, an A/D sampling rate up to about 200 MS/s is all that is needed for next-generation systems. As the speed of computers increases, the need for faster A/D's will increase

correspondingly. Those applications in the second group could benefit right now from A/D's with sampling rates in excess of a GS/s.

Some potential users at Wright Labs (Sharpin And Lutz) expressed a need for 6-8 bit A/D converters with a wide dynamic range. Such applications involve the passive monitoring of the microwave spectrum (such as in ELINT) where jamming is not a major issue.

We also identified an application in our company for high-speed, low-resolution A/D converters that is discussed in the next Section.

5.2 A Proposed AlliedSignal Application

One of our divisions is examining a digital anti-jamming receiver that would detect a number of satellite signals. The total bandwidth of the receiver is 400 MHz. Sampling at the Nyquist rate - and allowing extra bandwidth to account for roll-off in the bandpass filters - will require an A/D with about a 1.2 GS/s sampling rate. The signals to be sampled are spread spectrum. Because of the compression gain that occurs when the information is extracted from these spread-spectrum signals, we estimate that only four bits of resolution are required in the A/D converter. These specifications are well within the goals of our current program.

5.3 Proposed Manufacturing Plan

AlliedSignal maintains a complete materials growth and wafer fab facility at our Microelectronics and Technology Center. Except for e-beam lithography, which was contracted from three outside sources, the InP wafers processed under this program

were fabricated in this facility. We are currently bringing up an e-beam lithography process in house that will give us the capability of prototyping parts in small quantities. Since this is a research facility with single-wafer processing equipment, we would not expect production-like yields or throughputs. Fabrication of any significant number of A/D converters would involve either setting up a small pilot production line internally, or working with an existing InP foundry to transfer our A/D process technology to them.

Co-located with our III-V research labs is a Class 10 Silicon Fabrication Facility. This facility is a 1.2 micron CMOS fab. While we would not be able to run InP parts on this line due to possible cross-contamination issues (as well as wafer size problems -- the Si line is set up for 100 mm diameter wafers), there is room in the building to set up an InP line. A rough estimate of the cost involved, considering Hughes InP pilot line costs, would be on the order of $17 M. This includes the cost of MBE and E-beam lithography equipment, the two pacing pieces of equipment needed for our A/D converter process. It assumes that we dedicate one of our existing ion implanters to InP. We would, of course, need to evaluate the return on this level of investment before committing to build the fab based on existing and projected markets for these and other parts.

A less expensive alternative would be to transfer our A/D converter process to an existing InP foundry. We have contacted both Martin Marietta(Syracuse) and Hughes Research Labs to investigate this possibility. Both organizations have InP pilot lines, with MBE and e-beam lithography in place. Neither, however, has developed the selective epitaxy growth technology needed to grow RTD and MODFET (or HBT) structures on a single substrate. Either of these facilities would be a suitable partner to bring our A/D converters into production.

Hughes Research Labs has considerable experience in the development of state-of-the art InP devices and circuits based on MODFET and HBT Technology. They have demonstrated MODFET-based low noise amplifiers operating at frequencies as low as S-band all the way up to W-band. They pioneered the development of InP-based HBT IC technology. Hughes' InP-based HBT ICs have demonstrated the highest frequency of operation for a digital IC(39.5 GHz), the highest gain bandwidth product linear IC(88 GHz), and a high performance, reliable HBT IC process(MTTF > 10^7 Hrs @ 125 ^{o}C). A sketch of the Hughes state-of-the-art 10,000 square foot Class 10 Clean Room is shown in Figure 5.1. This 14 bay facility houses approximately $17 M of equipment dedicated to the development and pilot production of InP-based HEMT and HBT devices and ICs.

Martin Marietta Laboratories(Syracuse) is a second foundry for InP MMICs. They began developing InP MODFET/MMIC technology in 1988, and have established world-record performance in low-noise and power devices. Their process is space flight qualified. Martin Marietta has developed InP MODFET MMICs for internal consumption as well as government agencies such as ARPA, NRL, and Phillips Labs. Martin's 5,000 square foot process facility is located in Syracuse, NY. It includes both stepper and e-beam lithography, a low damage ECR nitride passivation reactor, and a RIE InP via hole etcher. Table 5.1 outlines the process flow for InP Power MODFET/MMICs. This process contains all of the steps needed to fabricate our A/D converter. The facility has a maximum process capacity of 1,000 wafers/year/shift. With an average A/D converter chip size of 1.5 mm X 1.5 mm and an estimated overall RF yield of 20%, each processed wafer would yield about 350 good chips.

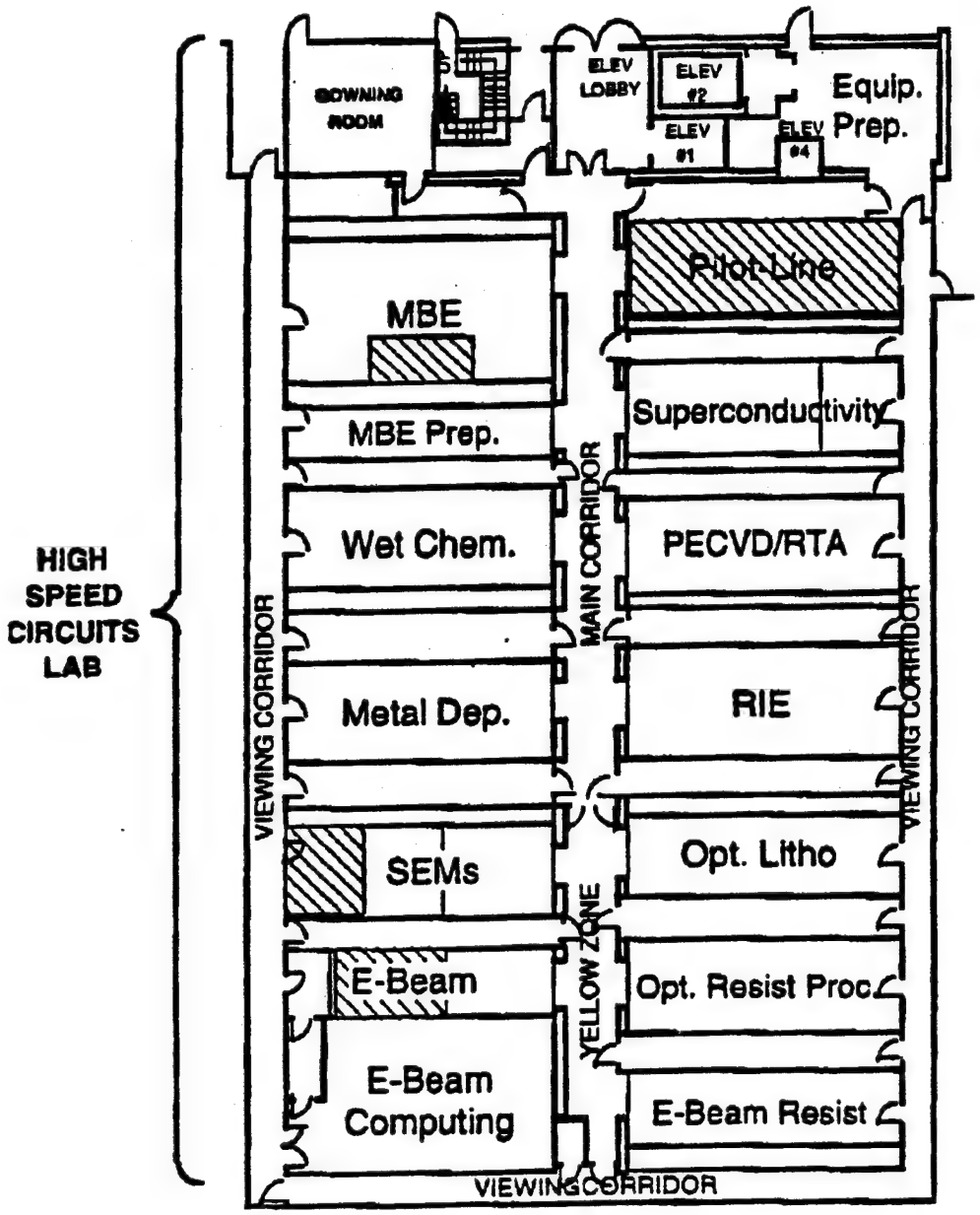


Fig. 5.1 Layout of the Hughes Research Lab high speed circuit laboratory.

Table 5.1. Process Flow for InP Power MODFET/MMICs

Front Side Process

Mesa Isolation	Wet chemically etched isolation to buffer layer
Ohmic Contact	AuGe thermally alloyed
Resistor Formation	TaN resistor
Gate Lithography	0.1, 0.15 and 0.25 μm x 3" E-beam lithography
Gate Recess	Low voltage SEM gate length inspection
	Selective gate recess can be used for uniformity and yield
Gate Metallization	Low resistance T-gate
Second Metallization	Further reduction of pad metal resistance
Dielectric Deposition	ECR Si_3N_4 passivation

Backside Process

Substrate Thinning	2-4 mil for MMICs (uniformity $\pm$ 5 μm)
Via-Hole Etch	Both wet and ECR RIE via hole etch available
Metallization	Au-based backside metal with excellent adhesion and reliability
Street Formation	To facilitate chip scribe and break
On-Wafer Testing	
Chip Separation	Scribe and Break

Once a decision is made to go into production of the A/D converter, AlliedSignal will meet with a InP foundry such as Hughes or Martin Marietta. We will either transfer our selective epitaxy process to them, or agree to supply starting wafers. Working with the foundry, we will jointly determine a suitable processing sequence, and design and lay-out an optimized mask set for the converters. As of this time the costs involved cannot be determined; cost sharing will be proportionate to the business interests of each company involved. We do expect that a substantial development effort will be required to bring these circuits to production lay-out an optimized mask set for the converters. As of this time the costs involved cannot be determined; cost sharing will be proportionate to the business interests of each company involved. We do expect that a substantial development effort will be required to bring these circuits to production.

6.0 Conclusions

Novel A/D converters based on the folding characteritics of the resonant tunneling diode were invented, fabricated, and tested. The monolithic fabrication of the RTD-based A/D converter represents the most complex InP-based integrated circuit demonstrated to date. Analog-to-digital conversion based on the *folding* characteristic of the multi-peaked RTD is practical for up to 4-bits of resolution and the circuit complexity is proportional to the number of bits of resolution; for greater resolution, the circuit complexity doubles for each bit above 4. The parallel nature of the RTD-based A/D converter makes it extremely fast, and the unique I-V characterisitcs of the multi-peaked RTD reduces the circuit complexity resulting in low-power A/D converter with an ultra-high sampling rate. Hysteresis in the RTD I-V characteristic limits the folding approach to A/D conversion to 4-bits. However, sigma-delta and subranging techniques can be used to make A/D converters that achieve resolutions of up to 8-bits at sampling rates of hundreds of MHz with our 4-bit A/D converter serving as the basic building block. High-speed, on-wafer testing is practical at sampling rates up to 3 GHz, however; for testing at higher sampling rates, mounting (wire bonding) the die/circuit in a fixture is a must.

We developed a selective epitaxial growth process to monolithically integrate GaInAs/AlInAs MODFET and RTD heterostructures on a single InP substrate. Our pioneering effort in this area should permit others to grow similar, high-quality, dual-heterostructure wafers. A complete double metal process technology was developed to fabricate the RTD-based A/D converter. However, a manufacturing-quality cleanroom is needed for obtaining high circuit yield, and the gate lithography must be e-beam or projection in order to obtain a high-yield gate process at gate lengths of 0.5 um or less. Depending on the requirements of future A/D converters based on RTDs, and on the manufacturing facilities available, either MODFETs or HBTs could be used for the supporting circuitry.

The RTD-based A/D converter can be manufactured using existing InP production facilities. However, a facility for manufacturing the dual heterostructure wafers still needs to be identified.

7.0 Recommendation for Future Work:

Our demonstration of a fully functional 5-bit A/D was the most significant achievement of this program. This also demonstrates the basic concept for using RTDs for A/D converters to dramatically improve their performance. What is needed now is to push this technology to real-system applications. These applications require sampling rates of 10 GS/s (or higher) and resolutions of 6-bits or higher.

In the course of our program, we identified several technological barriers that need to be overcome before this technology can be used for real applications. The first limitation is the compatibility of the low breakdown voltages of GaInAs/AlInAs MODFETs with the voltage required to span four peaks in the RTDs I-V characteristics. Replacing the GaInAs/AlInAs MODFET with a different, higher breakdown voltage device would allow more flexibility in RTD development . We have demonstrated an MBE-grown InP/AlInAs MODFET which has excellent millimeter-wave performance and a breakdown voltage (BV_{ds}) as high as 10V. The increased BV_{ds} would remove one important constraint in the design of the RTDs to meet the needs of the circuits. A second approach would be to replace the MODFET with HBTs. HBTs offer higher voltage gains, greater linearity, better threshold control and higher breakdown voltages. They also are capable of much higher current densities, which allows reduced device size, an important factor where packing density is important. The main drawback associated with InP HBTs are they are more difficult to process, particularly high performance, smaller emitter size devices.

The speed of the A/D is limited by the current-to-capacitance ratio of the RTDs and f_T of the transistor. Reducing the gate lengths of the MODFETs to 0.25 μm would result in a higher f_T at the expense of the BV_{ds}. Both the MODFET and HBT structures and

processing of these devices need to be optimized to simultaneously increase the f_T and breakdown voltage. In addition to the complex requirements of the RTD (sec 2.3), the RTD structure needs to be further optimized to reduce its voltage span to meet the needs of the circuit. We believe from our recent experiments under our IR&D program that we can reduce the voltage required to span four peaks in the RTD I-V characteristics. By using antimony-containing heterostructures, we can not only reduce the voltage span but also achieve a higher current-to-capacitance ratio for the RTD.

The trade-off between using lower-speed, higher-resolution A/Ds and higher-speed, lower-resolution A/Ds depends on the dynamic range needed to accomplish the desired system performance. The RTD-based folding A/D converter falls into the category of higher-speed, lower-resolution A/Ds, because of its limited 4-bit resolution. We need to develop ways for extending the resolution and accuracy of the A/D to the 10-14 bit range. For example, subranging, recursive, and Σ-Δ approaches for increased resolution should be investigated. We used depletion mode logic for the buffer amplifier, which results in high power dissipation. We need to optimize the design of the buffer amplifier to reduce power consumption, possibly by going to enhancement/depletion (E/D) mode logic. This approach would minimize the number of power supplies needed.

Achieving higher-speed sampling (10 GS/s or higher) with four bits (or higher) resolution will require processing the wafers on a InP production line. Such pilot lines are beginning to emerge and are discussed in Section 5.0. An InP-HBT or MODFET foundry needs to be selected and our growth and processing procedures should be transferred to the foundry.

In the A/D program, we were limited by on-wafer testing to speeds less than 3.0 GHz. Another issue not addressed in this program was modeling the effect of all the parasitics associated with the chip and packaging of ultra-high speed A/D. Both the on-wafer testing and packaging need to be addressed.

All of the issues addressed above are engineering issues that will be solved with further development effort. Of all the approaches for high-speed A/D's that have been proposed by ourselves and others, the RTD-based approach offers the best opportunity to achieve sampling rates of 10 GS/s or better at levels of power consumption acceptable to the typical user.

8.0 Appendix

8.1 References, Publications, and Presentations

8.1.1 References

1. A. Arbel and R. Kurz, 'Fast ADC,' *IEEE Trans. Nucl. Sci.* **NS-22**, 446 (1975).

2. T.H. Kuo, H.C. Lin, R.C. Potter, and D. Shupe, 'Novel A/D Converter Using Resonant Tunneling Diodes,' *IEEE J. Solid-State Circuits* **26**, 145 (1991).

3. S.-J. Wei, H.C. Lin, R.C. Potter, and D. Shupe, 'A Self-Latching A/D Converter Using Resonant Tunneling Diodes,' *IEEE J. Solid-State Circuits* **28**, 697 (1993).

4. R.C. Potter, A. Fathimulla, D. Shupe, H. Hier, S.-J. Wei, and H.C. Lin, 'A Monolithic, Resonant Tunneling Diode-Based, Analog-To-Digital Converter Built on InP,' Proceedings of the 5th International Conference on InP and Related Materials (Post Deadline Papers), pp. 37-40, Paris, France, April 19-22, 1993.

5. T.H. Kuo, H.C. Lin, U. Anandakrishnan, R.C. Potter, and D. Shupe, 'Large-Signal Resonant Tunneling Diode Model for SPICE3 Simulation,' Proceedings of IEEE International Electron Devices Meeting, pp. 21.7.1-21.7.4, Decemeber 3-6, Washington, D.C., 1989.

6. H.C. Lin and W.N. Jones, 'Computer Analysis of the Double-Diffused MOS Transistor for Integrated Circuits,' *IEEE Trans. on Elect. Dev.* **ED-20**, 275 (1973).

8.1.2 Publications Resulting from this Contract:

S.-J. Wei, H.C. Lin, R.C. Potter, and D. Shupe, 'A Self-Latching A/D Converter Using Resonant Tunneling Diodes,' *IEEE J. Solid-State Circuits* **28**, 697 (1993).

R.C. Potter, 'Indium-Based Resonant Tunneling Diodes for Signal Processing Applications,' *J. Korean Physical Society* **26**, S27 (1993).

S.-J. Wei, H.C. Lin, R.C. Potter, and D. Shupe, 'Dynamic Hysteresis of RTD Folding Circuit and Its Limitation on an A/D Converter,' *IEEE Trans. on Circuits and Systems* **39**, 247 (1992).

T.H. Kuo, H.C. Lin, R.C. Potter, and D. Shupe, 'Novel A/D Converter Using Resonant Tunneling Diodes,' *IEEE J. Solid-State Circuits* **26**, 145 (1991).

8.1.3 Invited Talks Resulting from this Contract:

R.C. Potter, A. Fathimulla, H. Hier, D. Shupe, J. Abrahams, C. Eichner, and D. Jones, 'A Monolithic Analog-To-Digital Converter Using Resonant Tunneling Diodes,' **invited talk**, Proceedings of the 1993 International Semiconductor Device Research Symposium, pp. 313, 313a, 314, 314a, University of Virginia, Charlottesville, VA., December 1-3, 1993.

R.C. Potter, 'A Monolithic Resonant Tunneling Diode-Based Analog-To-Digital Converter,' **invited talk**, Proceedings of the XXIVth General Assembly of the International Union of Radio Scientists, Kyoto, Japan, August 25-Sept. 2, 1993, page 170.

R.C. Potter, 'Analog-To-Digital Conversion Using Resonant Tunneling Diodes,' **invited talk**, presented at the Advanced Heterostructure Transistor Workshop, Kona, Hawaii, Nov. 29 - Dec. 4, 1992.

R.C. Potter, 'In-Based Resonant Tunneling Diodes for Signal Processing Applications,' **invited talk**, presented at the 1992 International Symposium on the Physics of Semiconductor Applications, Seoul, South Korea, August 5-7, 1992.

8.1.4 Conference and Symposium Presentations Result from this Contract:

R.C. Potter, A. Fathimulla, D. Shupe, H. Hier, S.-J. Wei, and H.C. Lin, 'A Monolithic, Resonant Tunneling Diode-Based, Ananlog-To-Digital Converter Built on InP,' Proceedings of the 5th International Conference on InP and Related Materials (Post Deadline Papers), pp. 37-40, Paris, France, April 19-22, 1993.

P. Roblin, R.C. Potter, and A. Fathimulla, 'Interface Roughness Scattering in AlAs/InGaAs/AlAs Resonant Tunneling Diodes with InAs Subwell,' Proceedings of the 5th International Conference on InP and Related Materials, Paris, France, April 18-22, 1993.

S.-J. Wei, H.C. Lin, R.C. Potter, and D. Shupe, 'High Speed A/D Converter Using Resonant Tunneling Diodes,' presented at the 1992 International Symposium on Circuits and Systems, San Diego, CA, May 10-13, 1992.

A. Fathimulla, H. Hier, and J. Abrahams, 'Monolithic Integration of RTDs and MODFETs on SI-InP,' International Conference on MBE, Austin, Texas, October, 1991.

8.1.5 Theses Resulting from this Contact:

1. Tai Haur Kuo (Ph.D.) "Analog-to-Digital Converter Using Resonant Tunneling Diodes," University of Maryland, College Park, Department of Electrical Engineering, 1990. (Can be obtained from University Microfilm International, Ann Arbor, MI.)

2. Sen Jung Wei (Ph.D.) "Analog/Digital Circuit Applications Using Resonant Tunneling Diodes," University of Maryland, College Park, Department of Electrical Engineering, 1993. (Can be obtained from University Microfilm International, Ann Arbor, MI.)

3. Hao Tang (Masters) "Dynamic Testing of Ultra-High-Speed Ananlog-To-Digital Converters," University of Maryland, College Park, Department of Electrical Engineering, 1993.

8.2 Chronological Summary of Reports, Meetings and Significant Milestones

Date	Activity
Sept 90	Award of the contract N00014-90-C-028
Dec 90	1- and 2-bit test mask designed, ordered and received
Jan 90	Quarterly report for the period 01 Sept 94 to 30 Nov 90
Feb 90	RTD mask designed, ordered and received
March 90	Quarterly report for the period 01 Dec 90 to 28 Feb 91
June 91	Quarterly report for the period 01 March 91 to 31 May 91
Sept 91	Quarterly report for the period 01 June 91 to 31 Aug 91
Oct 91	New circuit for digitizer
Dec 91	Quarterly report for the period 01 Sept to 30 Nov 91
Feb 91	Submitted annual letter for the period 01 Oct 90 to 31 Dec 91
March 92	Quarterly report for the period 01 Dec 91 to 29 Feb 92
March 92	Program review with ONR/ARPA at MTC. Goals were changed from 4- and 8- bit A/D's to 3- and 6-bit A/Ds.
March 92	Selected RTD and MODFET structure
April 92	Review of A/D architectures and selection of A/D circuit for the design.
May 92	Layout of 1- and 3-bit A/Ds completed, mask ordered & received. Revised 2- mask levels
June 92	Quarterly report for the period 01 March 92 to 31 May 92
Sept 92	Quarterly report for the period 01 June 92 to 31 Aug 92
Oct 92	Presentation at Ultra Program, Santa Fe
Dec 92	Quarterly report for the period 01 Sept 92 to 30 Nov 92
Feb 93	Annual report for the period of 01 Oct 91 to 31 Dec 92
Mar 93	Quarterly report for the period 01 Dec 92 to 28 Feb 93
Mar 93	3- and 6-bit mask designed, layout completed and review with U of MD.
Apr 93	HBT/ADC review in Reston, VA
Apr 93	3- and 6-bit mask ordered and received
June 93	Quarterly report for the period 01 March 93 to 31 May 93
Sept 93	Quarterly report for the period 01 June 93 to 31 Aug 93
Oct 93	Revised the 3- and 6-bit mask.
Dec 93	Quarterly report for the period 01 Sept 93 to 30 Nov 93
Jan 94	Annual report for the period 01 Oct 92 to 31 Dec 93
March 94	Quarterly report for the period 01 Dec 93 to 28 Feb
Apr 94	Presentation at HBT/ADC Review in Reston, VA
Jun 94	Quarterly report for the period 01 Mar 94 to 31 May 94
Sept 94	Quarterly report for the period 01 June 94 to 31 Aug 94
Oct 94	Presentation at the Ultra Program, Sante Fe

8.3 Thesis Summary

ANALOG/DIGITAL CIRCUIT APPLICATIONS USING RESONANT TUNNELING DIODES

by

Sen-Jung Wei

Dissertation submitted to the Faculty of the Graduate School
of the University of Maryland in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
1993

Advisory Committee:

Professor Hung C. Lin, Chairman/Advisor
Professor P. S. Krishnaprasad
Professor Aristos Christou
Associate Professor Agisilaos Iliadis
(Allied-Signal) Dr. Robert C. Potter

Chapter 8

Conclusions

In conclusion, a current-mode RTD ADC based on InGaAs/InAlAs RTD and InGaAs/InAlAs MODFET technology is developed, fabricated and tested. The ADC is much simplified by the folding characteristic of RTD and the novel circuit structure proposed. The 3-bit ADC requires 3 digitizers for each bit using 2-peak RTD's. The 4-bit ADC requires 5 digitizers by using 2-peak RTD's. The digitizers number can be reduced by improving the peak number of RTD and the controllability of the negative differential resistance of RTD. A first integrated RTD ADC is successfully demonstrated. The ADC can operate up to 2 GHz sampling rate, which is limited by the speed response of the clock driver. The design issues related to the performance of the ADC is addressed by analyzing the dynamic hysteresis effect of RTD folding circuits. From the analysis, design guides for the intrinsic I-V curve of RTD and the bias circuit are established.

Different types of self-latching RTD ADC are also proposed and simulated. The advantages and disadvantages of different converter structures are investigated and the sensitivity of the performance of the converters to circuit and device nonidealities are examined.

The RTD has been considered to be a promising device in the applications of multi-valued circuits. The functionality of RTD circuit is increased due to its folding characteristic. Due to the fast switching speed of RTD, one can increase the signal swing to overcome the low noise margin problem of multi-valued circuits. A multi-valued SRAM cell, two multi-valued counters and a multi-valued adder are proposed and verified by breadboarding the circuit using discrete devices. The isolation problem of two-terminal devices is solved by implementing clocked switches at the I/O ports of the circuits.

ANALOG-TO-DIGITAL CONVERTER USING RESONANT TUNNELING DIODES

by

Tai-Haur Kuo

Dissertation submitted to the Faculty of the Graduate School

of The University of Maryland in partial fulfillment

of the requirements for the degree of

Doctor of Philosophy

1990

Advisory Committee:

Professor **Hung C. Lin**, advisor

Professor **Robert W. Newcomb**

Associate Professor **Nariman Farvardin**

Associate Professor **Ching-Ping Wang**

(Allied-Signal) Dr. **Robert C. Potter**

CHAPTER
SIX

CONCLUSION

The high speed A/D converter has traditionally been regarded as the exclusive domain of bipolar transistor technology. Recently, III-V compound material is used to replace Si in high-speed bipolar transistor technology. Much effort has been put on the development of the III-V heterojunction bipolar transistor (HBT). The HBT is thought to be the hope to push A/D conversion to higher speed. The highest speed A/D converter, a 4-bit 3GHz which is a flash type and implemented by HBT technology, has been reported for several years. Since the speed increase of the A/D converter is stunted in the existing Si and III-V transistor technology, the new concept for A/D converters based on RTDs is a candidate to breakthrough the speed bottleneck.

In addition, the RTD device design and its circuit design are more realizable, controllable, and conceivable through the presented analysis of its hysteresis and I-V characteristics (Chapter 3). The computer simulation of complex circuits which contain RTDs can be done since a large-signal RTD model has

been proposed to be used with existing SPICE3 device models (Chapter 4). This make system which contain RTD circuits more predictable.

In this dissertation, a new concept for A/D converters based on RTDs is described. This approach holds promise for greatly increased speed and reduced circuit complexity in comparison to state-of-the-art flash A/D converters. The results from the theoretical analysis presented, the breadboard circuit demonstration, and the SPICE3 simulation results are very encouraging. In order to implement this new concept, the circuit design of high-speed buffers and subtracters based on the InGaAs/InAlAs MODFET [FAL] have been developed to support the inherently fast response of the RTD circuit. The process, device, and layout design are in progress at Allied-Signal Aerospace Technoogy Center led by Dr. Potter.

A multiple-valued counter [KL4], which can be used as peripheral circuit of an RTD-based system, is described in Appendix-B.

Future work will be emphasized on MODFET modeling, circuit optimization, struceure design of ADC, and prerformance evaluation.

DYNAMIC TESTING OF ULTRA HIGH SPEED ANALOG TO DIGITAL CONVERTERS

by

Hao Tang

Thesis submitted to the Faculty of the Graduate School
of The University of Maryland in partial fulfillment
of the requirements for the degree of
Master of Sciences
1993

Advisory Committee:

Professor Jung C. Lin, Chairman/Advisor
Associate Professor Charles Silio
Assistant Professor Linda Milor

CHAPTER SIX

CONCLUSION

The ultra high frequency sampler have been successfully designed and assembled. In addition, the existing testing software was modified for better adaptability to the new testing system. Initial test results have shown that our ultra high speed sampler is functioning properly by itself. When interconnected with the A/DC or systems with a different ground system, the waveform displays a few glitches (Fig. 5.3a). One possible source of this sparkle code is due to phase noise of the counter which in turn is thought to be generated by the paracitic inductances in junction with the transient currents. This is also commonly referred to as ground bounce. The voltage noise is also thought to be caused by the high speed switching nature of the GaAs digital circuits. Currently, we are further investigating into the possibility of reducing some of the transient noises by a unified ground system for both the test fixture and UUT.

In conclusion, we have demonstrated a simple, inexpensive method of testing A/DCs with up to 4 bits and sampling rate over 1

GHz. The operational speed can also be upgraded easily with faster chips which is readily obtainable by the use of GaAs MESFET technology. The Effective Number of Bits parameter can be carried out via histogram testing method, since this method can be effectively used when undersampling with beat frequency is the case in ultra high speed test conditions. This A/DC testing technique holds promise for reducing the high cost nature in today's high bandwidth A/DC or mixed signal testers.